IAA Correlator Center

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Abstract

The 12-board correlator MicroPARSEC equipped with S2-PT terminals was completed in 2007. This correlator is used for processing up to 3-station observations. The new correlator ARC for 6-station VLBI observations processing is under development. The VLBI data of the 3-station observations of the Russian national network Quasar was processed using MicroPARSEC correlator.

1. Introduction

The IAA Correlator Center is located and staffed by the Institute of Applied Astronomy in St.-Petersburg, Russia.

The IAA Correlator Center is devoted to processing geodetic, astrometric, and astrophysical observations made with the Russian national VLBI network Quasar.

2. Summary of Activities

2.1. MicroPARSEC Correlator Development

In 2007 the 12-board correlator MicroPARSEC was finished (Figure 1). It is capable of processing simultaneously up to 24 frequency channels to a maximum of 32MHz clock frequency and 2-bit sampling. The correlator is designed to process 2- or 3-station VLBI observations of 16 frequency channels from each station. If handling 3-station experiments, then 3 baselines of 8 frequency channels each are processed simultaneously.

At present the correlator is used for processing VLBI observations for astrometry. As a result, the correlator produces accurate geometric delays stored in NGS files.

Special PCI-standard boards called "MicroPARSEC units" are the main component of the MicroPARSEC correlator. Each unit is designed based on the Altera FPGA technology and contains two XF correlation devices. These units are placed into a special industrial computer (Figure 2).

Currently the correlator is equipped with two S2 playback terminals. In 2008 we are planning to equip it with Mark 5B terminals.

2.2. ARC Correlator Development

A new correlator ARC (Astrometric Radiointerferometric Correlator) development was started in 2007. This correlator will be able to process VLBI signals from 6 station (15 baselines) with 16 frequency channels each simultaneously. The correlator will have 2-bit sampled VSI-H signals at 32MHz maximum clock on its input. The maximum data rate of each station would be 1 Gbit per second. We are planning to equip this correlator with Mark 5B terminals.

The main processing device of ARC is BMC (Basic Module of Correlator), which is very similar to the MicroPARSEC unit (Figure 3). It is designed with FPGA technology in PCI board standard. The XF correlation algorithm is applied. All mathematical algorithms are FPGA's code.

Figure 1. 12-board MicroPARSEC correlator.

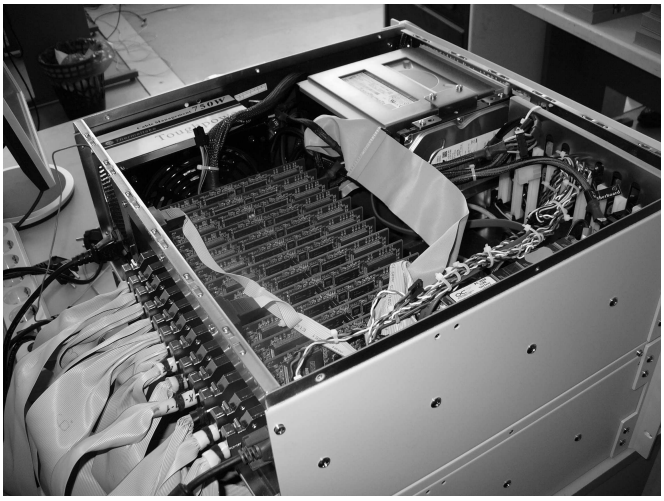

Figure 2. Industrial computer chassis with 12 MicroPARSEC units.

In comparison with MicroPARSEC unit, BMC has a larger size. It is Compact PCI 6U device. Also BMC has a greater number of correlation devices—16 instead of 2 in MicroPARSEC unit. Each device represents a single-baseline, single-channel XF correlator for calculating 64 complex delays and picking out calibration signals. BMCs are inserted into the Compact PCI 6U crates.

The correlator includes 15 BMCs and 6 Mark 5B terminals. SDSS (Signals Distribution and Synchronization System) provides Mark 5B with synchronization signals (DPSCLOCK and DPS1PPS) and transmits VLBI data from Mark 5B to BMC (Figure 4). SDSS transfers data streams of each station to 5 BMCs.

BMCs carry out all hardware data processing. Each BMC receives data streams of 2 stations and processes 16 frequency channels per baseline.

The correlator hardware control software is distributed over 4 Compact PCI 6U crates with

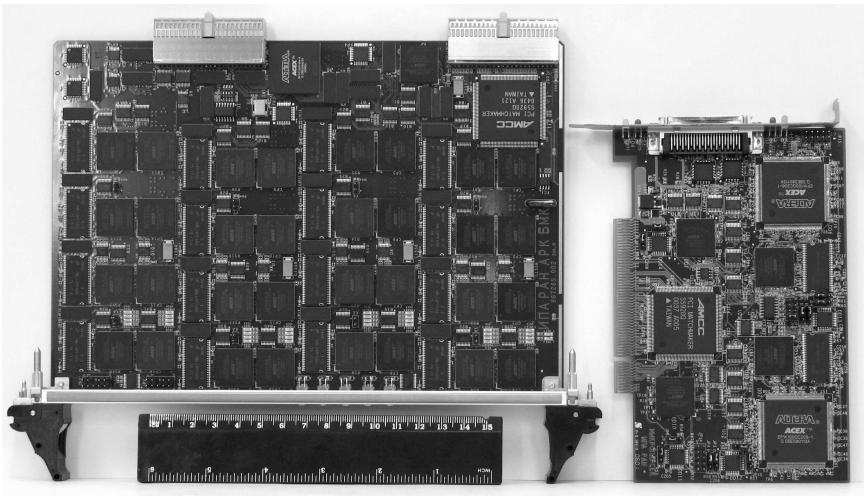

Figure 3. ARC BMC unit (left) and MicroPARSEC unit (right).

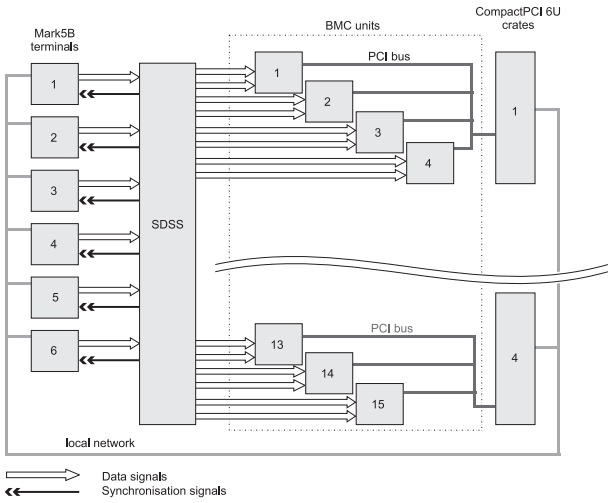

Figure 4. ARC correlator.

BMCs and a personal computer from where management is being carried out. Mark 5B terminal control, crates coordination, and data transfer are realized through the local correlator network.

At the present time the pilot batch of the BMCs have been produced. The correlator prototype construction has been started. We are planing to complete and test the full scale correlator in 2009.

3. Experiments Done

The regular national VLBI observations with the 3-station Quasar VLBI network were continued in 2007. Observational data were processed using the 4-board MicroPARSEC correlator (before February 2007) and 12-board MicroPARSEC correlator (since February 2007). All the

processed VLBI observations were 14 24-hour, 3-baseline sessions and 24 8-hour, single-baseline sessions.

The obtained group and ionospheric delay accuracy varies from 50 to 100 picoseconds.

4. Staff

- Andrey Bogdanov — software developer
- Artemy Fateev — software developer
- Alexey Melnikov — software developer, scheduler
- Violet Shantyr — software developer, post processing
- Igor Surkis — leading investigator, system integrator, software developer
- Vladimir Zimovsky — hardware developer, system integrator, correlator operator