On April 19, 2024, the Department announced a set of submission deadlines for pre-applications and full applications for our Notice of Funding Opportunity for Commercial Fabrication Facilities (NOFO). Please see the amended NOFO and our updated FAQs for more information, including submission deadlines.

CHIPS for America Guide **July 21, 2023**

Funding Opportunity – Commercial Fabrication Facilities
GUIDE: Statement of Interest

Submission of a statement of interest (SOI) is required to be eligible to submit a pre-application or an application.

Submitting an SOI does not obligate a potential applicant to submit a pre-application or an application. SOIs are not subject to merit review but will be used for internal planning purposes. The program office will use your SOI to gauge overall interest in the program, assess the types of projects and applicants who are interested in these funding streams, and estimate staffing for subsequent pre-applications and applications.

Your SOI must be submitted a minimum of 21 days prior to submitting a pre-application or full application. Refer to the CHIPS Incentives Program—Commercial Fabrication Facilities Notice of Funding Opportunity (CHIPS-CFF NOFO) Section IV.G. and the Frequently Asked Questions page on the CHIPS website for information on the SOI.

While the current NOFO only permits applications for the types of commercial fabrication facilities described in the NOFO, submissions of SOIs for future CHIPS NOFOs on semiconductor materials or equipment for which capital expenditures are less than $300 million and research and development facilities will be accepted at this time. Potential applicants should not expect to receive any feedback on their SOI other than a message confirming receipt. An organization may submit only one SOI for each expected application.

SOIs must contain the following information (submitted via the CHIPS Incentives Application Portal):

Potential Applicant Information

- **Potential Applicant Name**: Provide the legal name of the entity potentially applying for CHIPS Incentives.
- **Corporate Parent Name**: Provide the legal name of the corporate parent of the entity potentially applying for CHIPS Incentives.
- **Organization Website**: Provide a URL address for the applying entity's website (or corporate parent if entity does not have a website).
- **Have you registered for SAM.gov?**: Choose "Yes" or "No" from the dropdown menu to indicate whether the potential applicant has applied for an account in the federal government's System for Award Management (SAM.gov). Potential applicants are strongly encouraged to begin the process of registering for SAM.gov and obtaining a UEI as early as possible. While this process ordinarily takes between three days and two weeks, in some circumstances it can take six or more months to complete due to information verification requirements. CPO is unable to issue a CHIPS Incentive to an entity that lacks a UEI.
- **UEI # [Optional]**: If the entity has already received a Unique Entity Identifier (UEI) via SAM.gov, enter the number. If the entity has not yet received a UEI, leave this box blank.

- **Are there other entities (e.g., customers, suppliers, investors, advisors) you anticipate partnering with in a meaningful way?**: Choose "Yes", "No", or "Not Determined at this Time" from the dropdown menu to indicate whether the potential applicant anticipates partnering with other entities.
    - **Please describe any potential partners referred to above:** *(only if "yes" is selected)* Provide a description of the potential partners (maximum 1500 characters).
- **Contact Information**: Provide details necessary to reach the potential applicant's point of contact, including
    - **Title**: The official title of the point of contact at the applying entity
    - **Name**: The full name of the point of contact
    - **Email**: A business email for the point of contact associated with the potential applicant
    - **Phone**: A day-time phone number for the point of contact
    - **Mailing Address**: A business mailing address to reach the point of contact to include:
        - Street Address
        - City
        - State
        - ZIP Code
        - For foreign addresses, this will include equivalent information including Country

Project Information

- **Project(s) Description**: Provide a description of the construction, expansion, or modernization activities for each proposed facility at a single location, the resulting products that will be manufactured, information on the scale, size, and capacity of production, and any known timelines (maximum 1500 characters).
- **Product End Market Application**: Provide a description of the types of customers and end markets that will be served by the technology being produced by each proposed facility.(maximum 500 characters).
- **Site location**: Provide the City, State, and Zip Code where the proposed facility will be located. If the location has not yet been determined, leave blank and mark "Not determined at this time."
- **Project Type(s)**: Choose from the dropdown menu to indicate whether the project(s) proposes the construction of a new facility, the expansion or modernization of an existing facility, or both. Refer to section I.B.1. in the CHIPS-CFF NOFO for more information on Project Types.
- **Facility Type(s)**: Choose from the provided options to indicate the type(s) of facility or facilities proposed for this project. Select all options that apply. Refer to section I.B.1. in the CHIPS-CFF NOFO for details on each of the possible Facility Types.
    - **Leading-Edge Facilities** that utilize the most advanced front-end fabrication processes for logic, 3D NAND Flash, and Dynamic Random-Access Memory (DRAM) semiconductors.
    - **Current-Generation Facilities** that produce semiconductors based on 5 nm to 28 nm process technologies, and include logic, analog, and mixed-signal devices.

- **Mature-Node Facilities** that include logic and analog produced with process technologies above 28 nm, discrete semiconductors, optoelectronics, and sensors.
- **Back-end Production Facilities** for the assembly, testing, or packaging of semiconductors that have completed the front-end fabrication process.
- **Wafer Manufacturing Facilities** for the high-volume production of semiconductor wafers, including wafers made from silicon, silicon carbide, and gallium nitride. These facilities are the sites of ingot production and wafer slicing, lapping, polishing, cleaning and inspection.
- **Semiconductor Materials and Manufacturing Equipment Facilities** (if project capital expenditures are greater than or equal to $300 million included in this NOFO, otherwise included in future NOFO)
- **Semiconductor Materials Facilities** for the manufacture or production, including growth or extraction, of materials used to manufacture semiconductors, which are the chemicals, gases, raw and intermediate materials, and other consumables used in semiconductor manufacturing.
- **Semiconductor Manufacturing Equipment Facilities** for the physical production of specialized equipment integral to the manufacturing of semiconductors and subsystems that enable or are incorporated into the manufacturing equipment.
- **Research & Development Facilities** (included in future NOFO)
- **Other:** if "other" is selected for Facility Type, provide a description for the facility in the space provided

- If the project includes a Leading-Edge Facility, a Current-Generation Facility, a Mature-Node Facility, or a Back-end Production Facility, a second question will appear for each selection regarding the technology type of the facility.
  - If Leading-Edge Facilities is selected, choose one of the following Technology Type options. If "Other" is selected, please specify the technology type:
    - Logic (below 5nm processes)
    - 3D NAND Flash Memory (200 layers or above)
    - Dynamic Random-Access Memory (DRAM) (half-pitch of 13nm and below)
    - Other
  - If Current-Generation Facilities is selected, choose one of the following Technology Type options. If "Other" is selected, please specify the technology type:
    - Logic (between 5nm and 28nm processes)
    - Analog (between 5nm and 28nm processes)
    - Mixed-Signal (between 5nm and 28nm processes)
    - Other
  - If Mature-Node Facilities is selected, choose one of the following Technology Type options. If "Other" is selected, please specify the technology type:

        - Logic (above 28nm processes)
        - Analog (above 28nm processes)
        - Discrete semiconductors
        - Optoelectronics
        - Sensors
        - Other
    - If Back-end Production Facilities is selected, choose one of the following Technology Type options. If "Other" is selected, please specify the technology type:
        - Advanced Packaging
        - Other
    - If Semiconductor Materials and Manufacturing Equipment Facilities is selected, provide a description of the primary materials or equipment that will be produced at the facility (max. 100 words)

- **Expected Total Capital Expenditures for all proposed projects**:
    - Provide an estimated range of total capital expenditures for all proposed projects (provide minimum and maximum). Total capital expenditures refers to expenses incurred in the construction or improvement of physical assets, such as the costs of land, building and construction, equipment and installation, physical improvements, and working capital during the construction phase. Potential applicants should provide the estimated range on a best-effort basis; figures provided are expected to be preliminary high-level estimates and should be refined with greater detail in future application steps.
    - Potential applicants may optionally provide commentary on the estimated Total Capital Expenditures for all proposed projects range, which could include a description of the key cost drivers, an explanation if the range provided is large, or other supporting details; if the proposed application is expected to include more than one project, information should be provided for each project, to the extent feasible (maximum 500 characters).
- **Estimated peak monthly unit production capacity:** provide an estimated number of units produced when the facility reaches peak production. Specify what the units being produced are (e.g., wafers, components).
    - If the facility will not have any production capacity, leave the box blank and select "Not Applicable."

CHIPS Application Information

- **Do you expect your next submission to be a pre-application or full application?:** select either pre-application or full application depending on which the potential applicant plans to submit next. Submitting a pre-application is recommended, with the exception of applications for leading-edge facilities.
- **Expected Timeline for Next Submission**: Estimate the date the potential applicant intends to submit a Pre-Application or Full Application by selecting a Month and Year. The applicant will not be required to submit their pre-application or Full Application at this date; this information is used for CPO to appropriately prepare for reviews. The Pre-Application or Full Application must be submitted a minimum of twenty-one days following the submission of the SOI.

- **Is there other information about the potential application that we should know? (optional)**: Provide any relevant information about the project or application (maximum 1500 characters).