(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 December 2010 (09.12.2010)

PCT

(10) International Publication Number
WO 2010/141318 A1

(51) International Patent Classification:
H01R 12/00 (2006.01)

(21) International Application Number:
PCT/US2010/036397

(22) International Filing Date:
27 May 2010 (27.05.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/183,378 2 June 2009 (02.06.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: COMPLIANT PRINTED CIRCUIT PERIPHERAL LEAD SEMICONDUCTOR TEST SOCKET

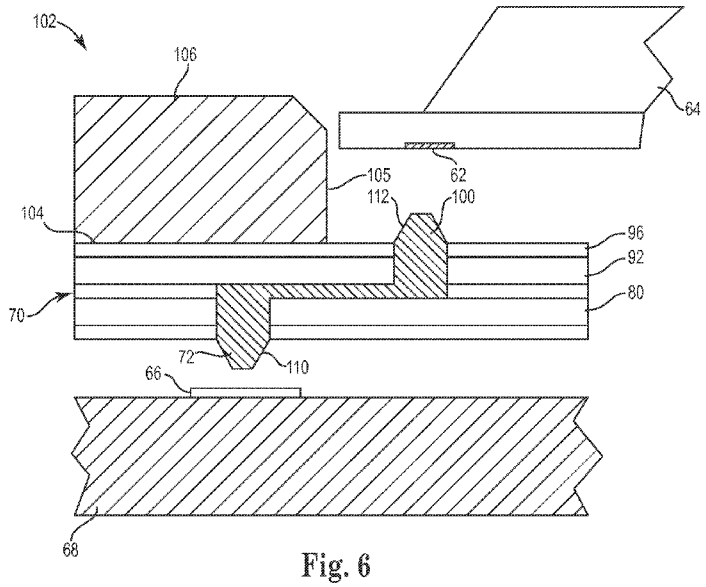

Fig. 6

(57) **Abstract**: A test socket that provides a temporary interconnect between terminals on an integrated circuit (IC) device and contact pads on a test printed circuit board (PCB). The test socket includes a compliant printed circuit and a socket housing. The compliant printed circuit includes at least one compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of conductive traces electrically coupling the first and second contact members. The compliant layer is positioned to bias the first contact members against the terminals on the IC device and the second contact members against contact pads on the test PCB. The socket housing is coupled to the compliant printed circuit so the first contact members are positioned in a recess of the socket housing sized to receive the IC device.

WO 2010/141318 A1

Attorney Docket No. 49956/601

COMPLIANT PRINTED CIRCUIT PERIPHERAL LEAD SEMICONDUCTOR TEST SOCKET

Field of the Invention

[0001] The present disclosure relates to a high performance electrical interconnect between an integrated circuit and a printed circuit assembly, and in particular, to a peripheral lead semiconductor test socket.

Background of the Invention

[0002] Traditional peripheral lead integrated circuit (IC) test sockets are generally constructed of a machined engineering grade plastic housing and frame, which is populated with a series of contact members that correspond to the terminals on two or four sides of the IC device. These contacts provide a temporary connection between the IC device terminals and the appropriate location on a test printed circuit board (PCB), also called a test or load board. This temporary electrical connection provides the mechanism to power the IC device and test performance.

[0003] The IC devices are graded based upon performance, and the devices that pass are identified while the devices that fail are either retested or discarded. In many cases, the performance windows in which the IC devices must operate can be fairly precise. Accordingly, the electrical performance of the contact members in the socket are important so as to not introduce degradation in signal or power delivery. A socket with good electrical performance is critical for many IC testing functions since poor performance can result in retesting or discarding devices that are actually acceptable but failed the test due to degradation within the socket.

[0004] IC manufacturers and their sub-contractors test millions or even billions of devices, and it is important for the socket to not only perform well electrically, but to also be mechanically robust enough to last hundreds of thousands of test cycles before being replaced. Many of the traditional sockets utilize very small metal contacts that are biased using elastomers. These contact members are mechanically compressed as the device is pushed against the contacts. An elastomeric material functions like a spring and provides the normal force to return the contact to the original position. The elastomeric material functioning as a spring member allows the contact members to be much shorter than they otherwise would

have to be in order to fashion a spring in conjunction with a contact member. The short length provides an electrical path that has fewer distortion effects as the current or signal passes through the contact. In some cases, spring probes are used which contain opposing metal contacts that are biased by a coil spring.

[0005] There are a wide range of contact types used in traditional sockets. In general, they all have a range of mechanical life that is limited by the effects of contacting the solder that is plated onto the terminals of the IC device. As the solder collects on the tips of the contacts, the Tin within the solder oxidizes to form a high resistance layer that causes the contact to lose electrical performance.

[0006] In some cases, the contacts move with respect to the interface to the circuit board as the device actuates the contact. This movement can cause wear on the PCB which can degrade performance of the circuit board. In general, the need for thousands of cycles before replacement drives sophisticated design that can be expensive. The socket volumes can also be relatively small requiring custom production methods that can also be expensive. The methods used to produce the plastic socket housings which hold the contacts are typically expensive precision machining operations. Many of the sockets are assembled by hand, where the elastomeric members and contacts are inserted by hand under magnification.

[0007] Socket users typically look for the best mix of electrical performance, yield, cost, and mechanical life to determine the costs to test each IC device. Electrical performance can be a hurdle that eliminates many of the socket options. Those sockets that can pass the electrical performance requirements can be limited by cost or the amount of use before they must be repaired or replaced. It can take hours or days to replace the failing socket, with the corresponding unit volume of IC devices which could have been tested being a major factor in the overall cost of use (*e.g.*, an opportunity cost). Damage to the PCB used for the test interface can also dramatically impact the cost of use as the PCB's can be very expensive and have a long lead-time to build (and replace).

Brief Summary of the Invention

[0008] The present disclosure is aimed at a test socket that is inexpensive to produce, has relative long life and provides excellent electrical performance.

[0009] The present disclosure leverages the capabilities of precision additive printed circuit fabrication techniques to create a compliant printed circuit that is designed to interface to a test board and make temporary electrical contact to the

terminal on an IC device. In basic terms, contact points can be created and positioned in the desired location relative to the points of contact to the PCB and the IC device terminals. A series of printing and sintering techniques can be employed to create a very precise and short electrical path. The contact members can be supported and biased by compliant materials that can be printed in an appropriate location to provide the desired effect when compressed. The nature of the compliant printed circuit fabrication process allows for many electrical enhancements not possible with traditional socket fabrication and testing techniques.

[0010] The disclosed compliant printed circuit fabrication process can allow for very high frequency performance, as well as the addition of on-board electrical devices and circuitry planes that are not available with other test sockets. The production cost for test sockets in accordance with the present disclosure can be a fraction the cost of producing existing test sockets. Use of additive printing processes, such as for example to print electrical features, can reduce capital cost and lead time for building the present test sockets. The additive printing processes can also increase yields over conventional test sockets that rely on conventional lithography tools and masks.

[0011] Internal compliance of the entire test socket and of individual contact members on the compliant printed circuit greatly increases performance of the present test sockets. The ability to build multi-layer structures over a relatively large area can permit terminal pitch on the IC devices to be reduced. The addition of circuitry planes and electrical devices in the present test sockets can provide performance enhancements not available with current test sockets. The ability to add electrical devices, such as transistors and memory, to the present test socket can provide the opportunity to incorporate test intelligence, extending the use of legacy test equipment and improving test performance. The present test sockets can provide the opportunity to develop adaptive testing and to alter the IC devices during testing.

[0012] The use of additive printing processes can permit the material set in a given layer to vary. Traditional PCB and circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or

semi-conductive materials at precise locations to create a desired effect can provide advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer can greatly enhance electrical performance.

[0013] The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to recesses in a previously deposited layer. The use of additive printing processes permit conductive material, non-conductive material, and semi-conductive material to be deposited and positioned on a single layer.

[0014] In one embodiment, pre-formed conductive trace materials are located in the recesses. The recesses can be plated to form conductive traces with substantially rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the recesses. The conductive foil is sheared along edges of the recesses. The excess conductive foil not located in the recesses is removed and the recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0015] One embodiment of the present disclosure is directed to a test socket providing a temporary interconnect between terminals on an IC device and contact pads on a test PCB. The test socket can include a compliant printed circuit and a socket housing. The compliant printed circuit can include at least one compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of conductive traces electrically coupling a plurality of the first and second contact members. The compliant layer is positioned to bias the first contact members against the terminals on the IC device and the second contact members against contact pads on the test PCB. The socket housing is coupled to the compliant printed circuit so the first contact members are positioned in a recess of the socket housing sized to receive the IC device.

[0016] A base layer of a dielectric material can be optionally printed onto the first and/or second major surfaces of the compliant printed circuit. The compliant printed circuit can include at least one additional circuitry plane. The additional circuitry plane can be one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, or a flexible circuit.

[0017] The contact members can be formed from one of a curable conductive material, sintered conductive particles, or a platable material. In one embodiment, the compliant printed circuit extends beyond a perimeter edge of a socket housing. In another embodiment, a flexible circuit member that is electrically coupled to the conductive traces extends beyond a perimeter edge of the socket housing.

[0018] At least one electrical device can be optionally printed on the compliant printed circuit and electrically coupled to one or more of the conductive traces. The electrical device can be selected from one of a shielding, a near device decoupling, a capacitor, a transistor, a resistor, a filter, a signal or power altering and enhancing device, a memory device, an embedded IC, a RF antennae, and the like. The electrical device can be preferably positioned within the socket housing.

[0019] The present disclosure is also directed to a test socket for testing IC devices. The test socket can include a compliant printed circuit with at least one compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of conductive traces electrically coupling the first and second contact members. A socket housing can be coupled to the compliant printed circuit so the first contact members are positioned in a recess of the socket housing. An IC device can be positioned in the recess of the socket housing with terminals on the IC device compressively engaged with the first contact members. The compliant layer can bias the first contact members against the terminals on the IC device. A test PCB can be electrically coupled with the second contact members. The compliant layer can bias the second contact members against contact pads on the test PCB.

[0020] The IC device can be selected from one of a bare die device or a packaged IC device. A plurality of electrical devices can be preferably located in the test socket and electrically coupled to one or more of the conductive traces. The electrical devices can be preferably programmed to monitor performance of the IC device during a testing protocol.

[0021] In one embodiment, the test PCB can include a first test protocol and at least a second test protocol triggered by one or more of electrical devices located in the test socket. In one embodiment, a test protocol can signal the test PCB to modify the IC device.

[0022] The present disclosure is also directed to a method of making a test socket. A compliant printed circuit can be formed by printing a first base layer of a

dielectric material onto a surface of a fixture. A conductive material can be deposited into a plurality of cavities or recesses in the fixture, such as for example by printing. The conductive material can be processed to form a plurality of first contact members along a first major surface of the compliant printed circuit. A compliant layer can be printed on the first base layer. A plurality of conductive traces can be printed onto an exposed surface of the compliant layer and electrically couple a plurality of the conductive traces with a one or more of the first contact members. A plurality of second contact members can be formed along a second major surface of the compliant printed circuit. The compliant printed circuit can be removed from the fixture and positioned in a socket housing so that the first contact members are located in a recess of the socket housing.

[0023] The present disclosure is also directed to a method of testing an IC device using the test sockets disclosed herein. An IC device can be located in the recess of the socket housing so that terminals on the IC device can electrically couple with the first contact members. The compliant layer can bias the first contact members against the terminals on the IC device. Second contact members can be electrically coupled with pads on a test PCB. The compliant layer can bias the second contact members against contact pads on the test PCB.

[0024] The method can include monitoring performance of the IC device during a testing protocol. In one embodiment, the test PCB can include a plurality of testing protocols. The method can include applying a second test protocol in response to performance of the IC device during a first test protocol. In another embodiment, at least one electrical device can be printed on the compliant printed circuit to monitor performance of the IC device during a testing protocol. A second test protocol can be applied in response to a signal from the electrical devices printed on the compliant printed circuit. The second test protocol can optionally modify the IC device, such as for example by altering software embedded thereon.

[0025] The present disclosure is also directed to a method of adaptive testing of IC devices using the test socket of the present disclosure. Electrical devices on the test socket monitor performance of the IC device being tested and signal the test PCB to modify the test protocol accordingly. The test station can also be signaled to modify the IC device.

Brief Description of the Several Views of the Drawing

[0026] Figure 1 is a cross-sectional view of a fixture for making a test socket in accordance with an embodiment of the present disclosure.

[0027] Figure 2 illustrates contact members formed in the fixture of Figure 1.

[0028] Figure 3 illustrates a compliant layer added to the assembly of Figure 2.

[0029] Figure 4 illustrates conductive traces coupled to the contact members of Figure 3.

[0030] Figure 5 illustrates a second compliant layer, a dielectric layer, and a contact member added to the assembly of Figure 4.

[0031] Figure 6 is a test socket in accordance with an embodiment of the present disclosure.

[0032] Figure 7 is a test socket having additional functionality in accordance with an embodiment of the present disclosure.

[0033] Figure 8 is a test socket with redundant contact members in accordance with an embodiment of the present disclosure.

[0034] Figure 9 is a test socket with a common ground plane in accordance with an embodiment of the present disclosure.

[0035] Figure 10 is a test socket having adjusted contact height and lateral offset in accordance with an embodiment of the present disclosure.

[0036] Figure 11 is a test socket with relocated or rerouted contact members in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0037] The present test sockets can be used to test semiconductor and other electrical devices having contact-to-contact spacing (pitch) on the order of less than about 1.0 millimeter (1×10^{-3} meter), and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. Such fine pitch test sockets are especially useful for evaluating IC devices.

[0038] Figure 1 is a side cross-sectional view of a fixture 50 useful in making a test socket in accordance with an embodiment of the present disclosure. The fixture 50 can include a plurality of cavities 52 (or recesses) in the first surface 54. The locations of the cavities 52 are arranged in an array that corresponds to terminals 62 on an IC device 64 (see Figure 6). The cavities 52 can be formed using any of a variety of techniques, including but not limited to molding, machining, printing, imprinting, embossing, etching, coining, and the like.

[0039] In the illustrated embodiment, the cavities 52 include side surfaces 58 and generally flat bottom surface 60. The bottom surface 60 facilitates electrical coupling with terminals 62 on the IC device 64 and contact pads 66 on a PCB 68 (see Figure 6). Although the cavities 52 are illustrated as truncated cones or pyramids, a variety of other shapes can be used, such as for example, cones, hemispherical shapes, and the like.

[0040] A base layer 56 can be preferably positioned on first surface 54 of the fixture 50. In one embodiment, the base layer 56 is printed onto the first surface 54, while leaving the cavities 52 exposed. In another embodiment, the base layer 56 is applied to the first surface 54 before the cavities 52 are formed, and the cavities 52 are formed through the base layer 56. In yet another embodiment, the base layer 56 extends along the surfaces 58, 60 of the cavities 52. The base layer 56 can facilitate removal of the compliant printed circuit 70 (see Figure 6) from the fixture 50. The base layer 56 can be preferably a dielectric material that also acts as a carrier layer for the compliant printed circuit 70.

[0041] The fixture 50 can be constructed from a variety of materials, such as for example metal, plastic, ceramic, and composites thereof. In one embodiment, the fixture 50 is made from a resist material that can be dissolved to release a compliant printed circuit formed on the fixture 50. Making the fixture 50 from a dissolvable material permits contact members 72 (see Figure 2) formed in the cavities 52 to have a variety of internal features, undercuts, or cavities that are difficult or typically not possible to make using conventional molding or machining techniques, referred to herein as a "non-moldable feature." The cavities 52 are optionally coated with a material to facilitate release of the contact members 72 from the fixture 50.

[0042] Figure 2 illustrates contact member 72 formed in the fixture of Figure 1. As illustrated in Figure 2, conductive material 74 can be deposited in the cavities 52 to form contact members 72. In one embodiment, the conductive material 74 is a metallic powder that can be sintered to create the contact members 72 (see Figure 6). In another embodiment, the conductive material 74 can be a flowable, curable conductive material.

[0043] In one embodiment, inner surface 58, 60 of the cavities 52 can be optionally pretreated before deposition of the conductive material 74. For example, the inner surfaces 58, 60 can be coated with particles of rhodium and then sintered. The sintered rhodium is then coated with nickel or copper. In another embodiment,

the inner surfaces 58, 60 can be coated with a low friction material that facilitates removal of the contact members 72 (see Figure 6) from the fixture 50.

[0044] The conductive material 74 is preferably deposited in a first state and then processed to create a second more permanent state. For example, the metallic powder can be deposited in the cavities 52 and subsequently sintered, or a curable conductive material can flow into the cavities 52 and can be subsequently cured. As used herein "cure" and inflections thereof refers to a chemical-physical transformation that allows a material to progress from a first form (e.g., flowable form) to a more permanent second form. "Curable" refers to an uncured material having the potential to be cured, such as for example by the application of a suitable energy source.

[0045] Various methods for deposition of electronic materials may be used to deposit the conductive material in the cavities, such as for example, inkjet printing, screen printing, aerosol printing, printing through a stencil, flexo-gravure printing, and offset printing.

[0046] Also, the compliant printed circuit 70 and various structures described herein are preferably manufactured using printing technology, such as for example, inkjet printing, aerosol printing, screen printing, printing through a stencil, flexo-gravure printing, and offset printing, rather than traditional PCB fabrication techniques. Various methods of printing the compliant printed circuit and the electrical devices are disclosed in U.S. Pat. Nos. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are incorporated herein by reference. For example, conductive inks containing metal particles are printed onto the compliant printed circuit 58 and subsequently sintered.

[0047] A printing process can preferably be used to fabricate various functional structures, such as conductive paths and electrical devices without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on

virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0048] U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated herein by reference, teach using inkjet printing to make various electrical devices, such as resistors, capacitors, diodes, inductors (or elements which can be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistors (including, light emitting, light sensing or solar cell elements, field effect transistors, top gate structures), and the like.

[0049] U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference, teach using aerosol printing to create various electrical devices and features.

[0050] Printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semiconductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0051] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or teflon.

[0052] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0053] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g.

Kapton, available from Dupont located in Wilminton, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0054] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0055] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0056] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181 (Bridenbaugh et al.), which is incorporated herein by reference.

[0057] A protective layer can optionally be printed onto the electrical devices and features. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[0058] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present invention.

[0059] An inkjet print head, or other print head, preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0060] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[0061] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electropneumatic, electrostatic, rapid ink heating, magnetohydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0062] While inkjet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: premetered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air

knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; aerosol printing processes; and other similar techniques.

[0063] Figure 3 illustrates a first compliant layer 80 selectively applied to a surface 82 of the base layer 56. The compliant layer 80 can be preferably printed onto the surface 82 using a printing technology as previously described. A rear surface 84 of the conductive material 74 can be left exposed to permit subsequent processing, such as for example electrically coupling to the contact member 72.

[0064] Figure 4 illustrates dielectric layers 86 and conductive traces 88 deposited, such as by printing, on the top surface 90 of the first compliant layer 80. In one embodiment, the conductive traces 88 can be created by sintering or by printing a platable target that can be subsequently plated with a conductive material. In one embodiment, the plating can be optionally applied using printing technology. Digital images of the dielectric layers 86 and conductive traces 88 are printed directly on the surface 90, eliminating or reducing many of the lithography, plating, and etching steps used to manufacture conventional probes. The resulting compliant printed circuit 70 (see Figure 6) can provide high frequency capability.

[0065] Inkjet and other printing processes are additive in nature. The additive nature provides an excellent means to form layers of the compliant printed circuit 70 (shown in Figure 6), such as for example dielectric layers covering the electrical traces, power planes, ground planes, and the like. Printing processes such as inkjet printing can also be use to print desired functions or electrical devices directly on the compliant printed circuit 70 (see Figure 6), rather than mounting the electrical devices discretely. Digital images of the dielectric layers, conductive traces, and electrical devices and features can be printed directly on a surface of the fixture 50 or of a previously applied layer, eliminating or reducing many of the lithography, plating, and etching steps conventionally used. The resulting compliant printed circuit 70 (see Figure 6) can provide high frequency capability. Moreover, the inkjet printing process can reduce manufacturing production time and cost by orders of magnitude.

[0066] The use of additive printing processes can permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect can offer advantages in tuning impedance or adding electrical function on a given layer. Tuning performance

on a layer by layer basis relative to the previous layer can greatly enhance electrical performance.

[0067] The resulting conductive traces 88 preferably have substantially rectangular cross-sectional shapes. The use of additive printing processes permits conductive material, non-conductive material, and semi-conductive material to be simultaneously located on a single layer.

[0068] In one embodiment, recesses 87 (or trenches) formed in an applied layer, such as the compliant layer 80 and the dielectric layer 86, can permit control of the location, cross section, material content, and aspect ratio of the contact members 72 and the conductive traces 88. Maintaining the conductive traces 88 with a cross-section of 1:1 or greater can provide greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etch the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using recesses to control the aspect ratio of the conductive traces 88 can result in a more rectangular or square cross-section of the conductive traces 88, with a corresponding improvement in signal integrity.

[0069] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces can be transferred to the recesses 87. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 87. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 87, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 87.

[0070] In another embodiment, a thin conductive foil is pressed into the recesses 87, and the edges of the recesses 87 act to cut or shear the conductive foil. The process positions a portion of the conductive foil in the recesses 87, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses 87 for easy removal. Again, the foil in the recesses 87 is preferably post plated to add material to increase the thickness of the conductive traces 88 and to fill any voids left between the conductive foil and the recesses 87.

[0071] Figure 5 illustrates the remaining process of fabricating the compliant printed circuit 70 in accordance with an embodiment of the present disclosure. A second compliant layer 92 is positioned on exposed surfaces 94 of the dielectric layers 86 and conductive traces 88. The second compliant layer 92 and second dielectric layer 96 can be selectively deposited on the exposed surfaces 94 to permit creation of a contact member 100.

[0072] The contact member 100 can be preferably created using the techniques discussed in connection with contact member 72. In one embodiment, cavities 101 in the second compliant layer 92 and the second dielectric layer 96 can be filed with conductive material 74. A second fixture with second contact members 100, such as illustrated in Figure 2, can be positioned so the second contact members 100 bond with the conductive material 74 such as during sintering or curing.

[0073] Alternatively, a pre-fabricated contact member 100 can be bonded to the conductive trace 88. As used herein, "bond" or "bonding" refers to, for example, adhesive bonding, solvent bonding, ultrasonic welding, thermal bonding, or any other techniques suitable for attaching adjacent layers of a substrate.

[0074] In another embodiment, the compliant printed circuit 70 can be made in two portions, such as illustrated in Figures 3 and 4, and then bonded together.

[0075] Figure 6 is a test socket 102 in accordance with an embodiment of the present disclosure. The compliant printed circuit 70 is removed from the fixture 50 (shown in Figures 1-5). In the illustrated embodiment, the dielectric layer 96 can be bonded to a surface 104 of a socket housing 106 so that contact members 100 are positioned in a recess 105 formed by the socket housing 106. The IC device 64 can be positioned in the recess 105 so that terminals 62 on the IC device 64 align with the contact members 100.

[0076] Exposed surfaces 110, 112 of the contact members 72, 100, can be optionally plated, either before or after the compliant printed circuit 70 is installed in the socket housing 106. In another embodiment, the contact members 72, 100 can be deformed, such as for example by coining or etching, to facilitate engagement with terminals 62 on the IC device 64.

[0077] Although the present test socket 102 is particularly well suited for testing packaged IC devices, it can be used on a variety of other circuit members, such as for example, unpackaged integrated circuits, printed circuit boards, flexible circuits,

bare-die devices, organic or inorganic substrates, or any other device capable of carrying electrical current.

[0078] In operation, the IC device 64, the test socket 102 and a PCB 68 are compressively coupled so that the contact member 100 electrically couples with the terminal 62 and the contact member 72 electrically couples with a contact pad 66 on the PCB. A compliant layer 80 can bias the contact member 100 into engagement with the terminal 62, while the compliant layer 92 can bias the contact member 72 into engagement with the contact pad 66. The compliant layers 80, 92 can also permit the contact members 72, 100 to deflect and thereby compensate for non-planarity of the terminals 62 or the contact pads 66.

[0079] Figure 7 is an alternate test socket 150 with additional functionality built into the compliant printed circuit 152 in accordance with an embodiment of the present disclosure. One or more of the layers 154A, 154B, 154C, 154D, and 154E (collectively "154") can include additional functionality, such as for example, specialty dielectrics, ground planes, power planes, shielding layers, stiffening layers, capacitive coupling features, circuitry layers, and the like. The layers 154 can be printed or preformed and selectively bonded or non-bonded to provide contiguous material or releasable layers.

[0080] The additional functionality can also be provided by additional electrical devices 160, preferably positioned adjacent to a recess 172 of a socket housing 168 that receives the IC device 164. The electrical devices 160 can be shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded IC, RF antennae, and the like. The electrical devices 160 can be added as discrete components or printed onto one of the layers. The electrical devices 160 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

[0081] In a preferred embodiment, the electrical devices 160 are printed onto the compliant printed circuit 70. As previously explained, various methods of printing electrical devices are disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey

et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. Electrical devices that are typically located on a separate test station or on a test PCB 162 can be incorporated into the test socket 150, and thereby improve electrical performance. Electrical devices 160 can also be positioned within the socket housing 168.

[0082] In one embodiment, the compliant printed circuit 152 extends beyond a perimeter edge 176 of the socket housing 168. In one embodiment, an extension 170 including a flexible circuit member can be electrically coupled to the compliant printed circuit 152. In the illustrated embodiment, the compliant printed circuit 152 is electrically coupled to a test station 166 via the extension 170. Alternatively, the test PCB 162 can be electrically coupled to the test station 166.

[0083] The testing protocol can reside on the test PCB 162, the test station 166, or a combination thereof. Reference herein to the test PCB should be construed to encompass the test station, either coupled to the test PCB or directly to the compliant printed circuit.

[0084] In one embodiment, the electrical devices 160 monitor the testing of the IC device 164 and communicate feedback to test station 166. In one embodiment, the feedback signal from the electrical devices 160 can cause the test station 166 to alter the testing protocol based on the performance of the IC device 164. This can be referred to as adaptive testing. In one embodiment, the feedback signal from the electrical devices 160 can cause the test station 166 to alter the IC device 164, such as for example, by altering software resident on the IC device 164.

[0085] Figure 8 is a test socket 200 in accordance with another embodiment of the present disclosure. The compliant printed circuit 202 can include multiple contacts 204A, 204B (collectively "204") for each terminal 206 on an IC device 208. The redundant contacts 204 can increase reliability and permit Kelvin measurements, which require two separate contact points at the terminal 206 of the IC device 208 routed to separate pads 210A, 210B (collectively "210") on the test PCB 212.

[0086] Figure 9 is a test socket 220 with common ground plane 222 in accordance with another embodiment of the present disclosure. Grounding contact

members 224, 226 can be coupled to a common conductive trace 228 in the compliant printed circuit 230. The conductive trace 228 functions as a grounding plane 222. The grounding contact members 232, 234 can connect the ground plane 222 to a test PCB 236.

[0087] Figure 10 is a test socket 254 having adjusted contact height 250 and lateral offset 252, in accordance with an embodiment of the present disclosure. Figure 10 illustrates the adaptive capabilities of the present disclosure by showing an ability to adjust contact height 250 and lateral offset 252 of test sockets 254 . Increasing thickness 256 of one or both of the compliant layers 258A, 258B can permit the contact height 250 to be adjusted. Increasing the depth of the cavities 52 in the fixture 50 (see Figure 1) can also be used to modify the contact height 250. The printing technology used to create the compliant printed circuit 260 allows lateral offset 252 to be easily adjust. Consequently, compliant printed circuits in accordance with various embodiments of the present disclosure can be adapted for use in existing socket designs.

[0088] Figure 11 is a test socket 270 with relocated or rerouted contact members 272A, 272B (collectively “272”) in accordance with an embodiment of the present disclosure. The test socket 270 illustrates one of various routing options of contact members of a test socket. A compliant printed circuit 274 can permit the contact members 272 to be arranged in various configurations. In the embodiment of Figure 11, the compliant layer 276 can simultaneously bias the contact member 272A toward an IC device 278 and the contact member 272B toward the test PCB 280.

[0089] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the invention. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the invention.

[0090] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[0091] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the embodiments of the present invention are not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[0092] Other embodiments of the invention are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the invention, but as merely providing illustrations of some of the presently preferred embodiments of this invention. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the invention. Thus, it is intended that the scope of at least some of the present invention herein disclosed should not be limited by the particular disclosed embodiments described above.

[0093] Thus the scope of this invention should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred

embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A test socket providing a temporary interconnect between terminals on an integrated circuit (IC) device and contact pads on a test printed circuit board (PCB), the test socket comprising:

a compliant printed circuit including at least one compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of conductive traces electrically coupling the plurality of first contact members and the plurality of second contact members, the compliant layer positioned to bias the plurality of first contact members against the terminals on the IC device and the second contact members against contact pads on the test PCB; and

a socket housing coupled to the compliant printed circuit, the first contact members positioned in a recess of the socket housing sized to receive the IC device.

2. The test socket of claim 1, wherein the conductive traces of the compliant printed circuit comprise substantially rectangular cross-sectional shapes.

3. The test socket of claim 1, wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer of the compliant printed circuit.

4. The test socket of claim 1, further comprising a base layer of a dielectric material printed to be positioned on at least one of the first and second major surfaces of the compliant printed circuit.

5. The test socket of claim 1, wherein the compliant printed circuit comprises at least one additional circuitry plane.

6. The test socket of claim 5, wherein the at least one additional circuitry plane comprises one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, and a flexible circuit.

7. The test socket of claim 1, wherein the contact members comprise at least one of a curable conductive material, sintered conductive particles, and a platable material.

8. The test socket of claim 1, wherein the compliant printed circuit extends beyond a perimeter edge of the socket housing.

9. The test socket of claim 1, further comprising a flexible circuit member electrically coupled to the conductive traces and extending beyond a perimeter edge of the socket housing.

10. The test socket of claim 1, further comprising at least one electrical device printed on the compliant printed circuit and electrically coupled to one or more of the conductive traces.

11. The test socket of claim 10, wherein the electrical device is selected from one of shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded ICs, RF antennae, and the like.

12. The test socket of claim 10, wherein the electrical device is positioned within the socket housing.

13. The test socket of claim 10, wherein the electrical device is positioned adjacent a recess of the socket housing.

14. A test socket for testing integrated (IC) devices, the test socket comprising:

a compliant printed circuit including at least one compliant layer, a plurality of first contact members located along a first major surface, a plurality of second contact members located along a second major surface, and a plurality of conductive traces electrically coupling the plurality of first contact members and the plurality of second contact members;

a socket housing coupled to the compliant printed circuit, the plurality of first contact members positioned in a recess of the socket housing; and

a test printed circuit board (PCB) electrically coupled with the plurality of second contact members, the compliant layer biasing the plurality of second contact members against contact pads on the test PCB.

15. The test socket of claim 14 further comprising an integrated (IC) device positioned in the recess of the socket housing with terminals on the IC device compressively engaged with the plurality of first contact members, the compliant layer biasing the plurality of first contact members against the terminals on the IC device.

16. The test socket of claim 15 wherein the IC device is selected from one of a bare die device or a packaged integrated circuit device.

17. The test socket of claim 14 comprising a plurality of electrical devices located in the test socket and electrically coupled to one or more of the conductive traces.

18. The test socket of claim 17 wherein the electrical devices are programmed to monitor performed of the IC device during a testing protocol.

19. The test socket of claim 14 wherein the test printed circuit board comprises:

a first test protocol; and

at least a second test protocol triggered by one or more of electrical devices located in the test socket.

20. The test socket of claim 19 wherein the second test protocol signals the test printed circuit board to modify the IC device.

21. The test socket of claim 19 wherein the second test protocol modifies software located in the IC device.

22. A method of making a test socket comprising the steps of:

forming a compliant printed circuit comprising the steps of;

printing a first base layer of a dielectric material onto a surface of a fixture;

depositing a conductive material into a plurality of the cavities in the fixture;

processing the conductive material to form a plurality of first contact members positioned along a first major surface of the compliant printed circuit;

printing a compliant layer on the first base layer;

forming a plurality of conductive traces on an exposed surface of the compliant layer and electrically coupling the plurality of the conductive traces with a one or more of the plurality of first contact members;

forming a plurality of second contact members positioned along a second major surface of the compliant printed circuit;

removing the compliant printed circuit from the fixture; and

positioning the compliant printed circuit in a socket housing so the first contact members are located in a recess of the socket housing.

23. The method of claim 22, wherein forming the conductive traces comprises printing an electrically active ink onto an exposed surface.

24. The method of claim 22, wherein the conductive traces comprise substantially rectangular cross-sectional shapes.

25. The method of claim 22, further comprising printing a conductive material, a non-conductive material, and a semi-conductive material on a single layer of the compliant printed circuit.

26. The method of claim 22, wherein forming the plurality of conductive traces comprises:

positioning pre-formed conductive trace materials in recesses of in the compliant layer; and

plating the recesses of the base layer to form conductive traces with substantially rectangular cross-sectional shapes.

27. The method of claim 22, wherein forming the plurality of conductive traces comprises:

pressing a conductive foil into at least a portion of recesses in the compliant layer;

shearing the conductive foil along edges of the recesses;

removing excess conductive foil not located in the recesses; and

plating the recesses to form conductive traces with substantially rectangular cross-sectional shapes.

28. The method of claim 22, further comprising the steps of:

depositing a conductive material into a plurality of the cavities in the compliant layer;

processing the conductive material to form the plurality of second contact members positioned along the second major surface of the compliant printed circuit.

29. The method of claim 22, wherein the step of forming a plurality of second contact members comprises the steps of:

printing a second base layer of a dielectric material onto a surface of a fixture;

depositing a conductive material into a plurality of the cavities in the fixture;

processing the conductive material to form a plurality of second contact members; and

coupling the second contact members with the conductive traces on the compliant printed circuit so the second contact members extend along the second major surface of the compliant printed circuit.

30. The method of claim 22, further comprising the step of forming at least one additional circuitry plane in the compliant printed circuit.

31. The method of claim 22, further comprising electrically coupling a flexible circuit member to the compliant printed circuit and extending the flexible circuit member beyond a perimeter edge of the socket housing.

32. The method of claim 22, further comprising the steps of:

printing at least one electrical device on the compliant printed circuit; and

electrically coupling the electrical device to at least one contact member.

33. The method of claim 22, wherein the step of processing the conductive material comprises one of sintering, plating, and curing.

34. A method of testing an integrated (IC) device using the test socket of claim 1, the method comprising the steps of:

positioning an IC device in the recess of the socket housing such that terminals on the IC device electrically couple with the plurality of first contact members, the compliant layer biasing the first contact members against the terminals on the IC device; and

electrically coupling the plurality of second contact members with pads on a test printed circuit board (PCB), the compliant layer biasing the plurality of second contact members against the contact pads.

35. The method of claim 34, further comprising monitoring performance of the IC device during a testing protocol.

36. The method of claim 34, wherein the test PCB comprises a plurality of testing protocols, the method comprising applying a second test protocol in response to performance of the IC device during a first test protocol.

37. The method of claim 34, further comprising at least one electrical device printed on the compliant printed circuit monitoring performance of the IC device during a testing protocol.

38. The method of claim 37, further comprising applying a second test protocol in response to a signal from the electrical device printed on the compliant printed circuit.

39. The method of claim 34, further comprising modifying the IC device in response to testing of the IC device.

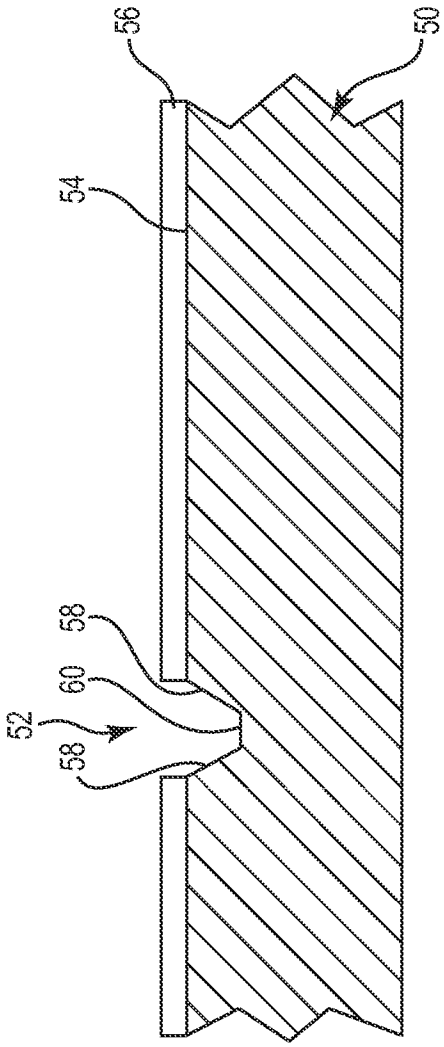

Fig. 1

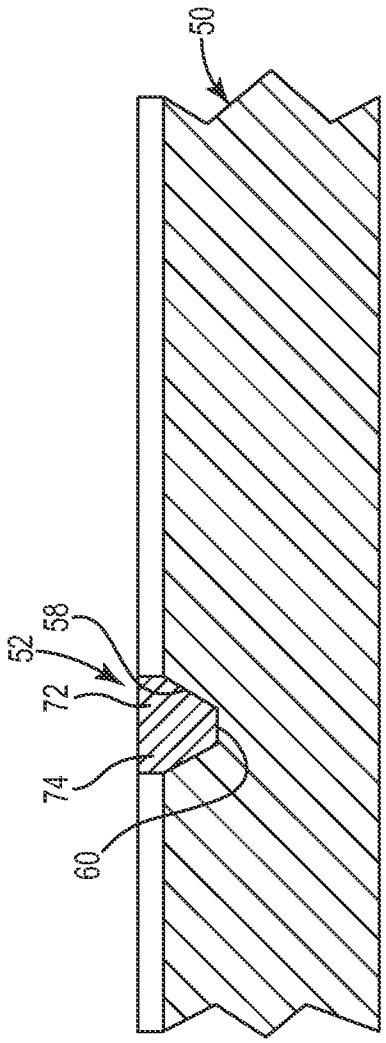

Fig. 2

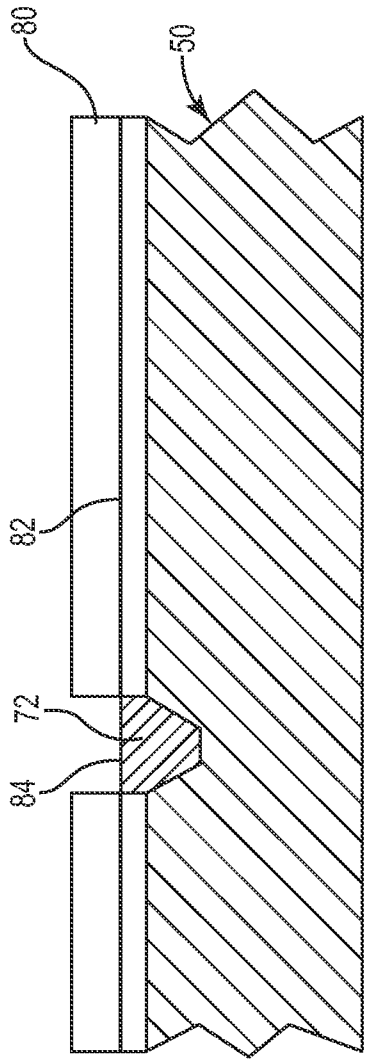

Fig. 3

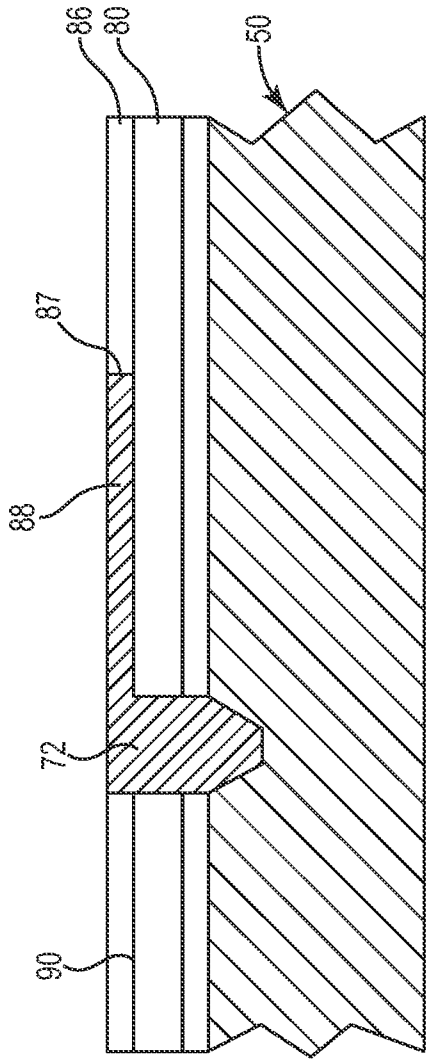

Fig. 4

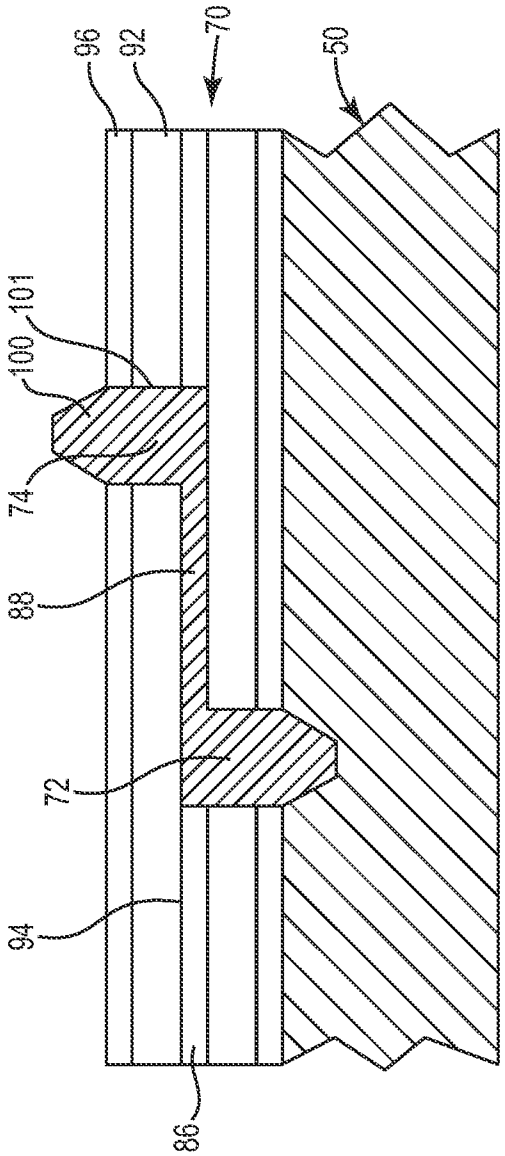

Fig. 5

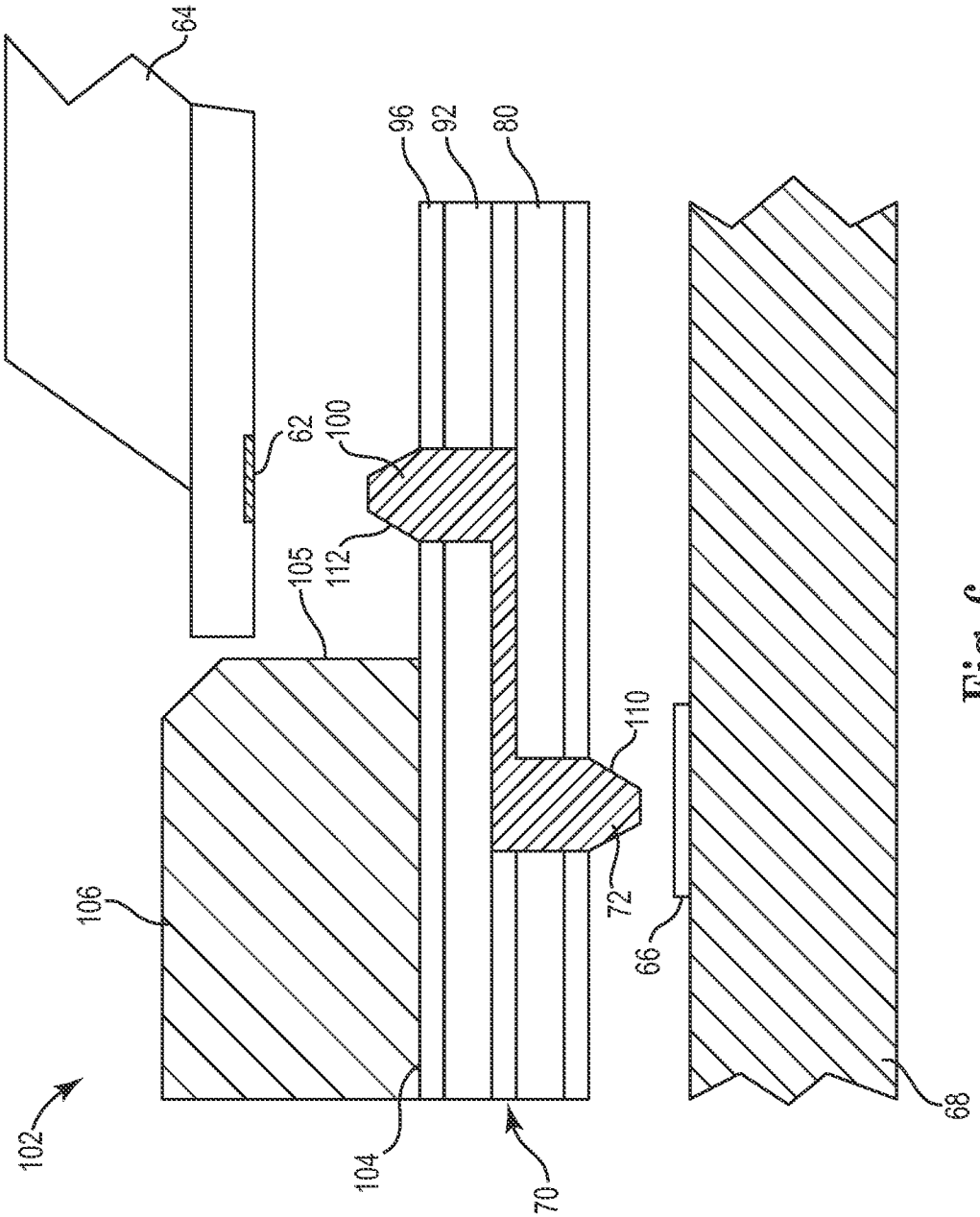

Fig. 6

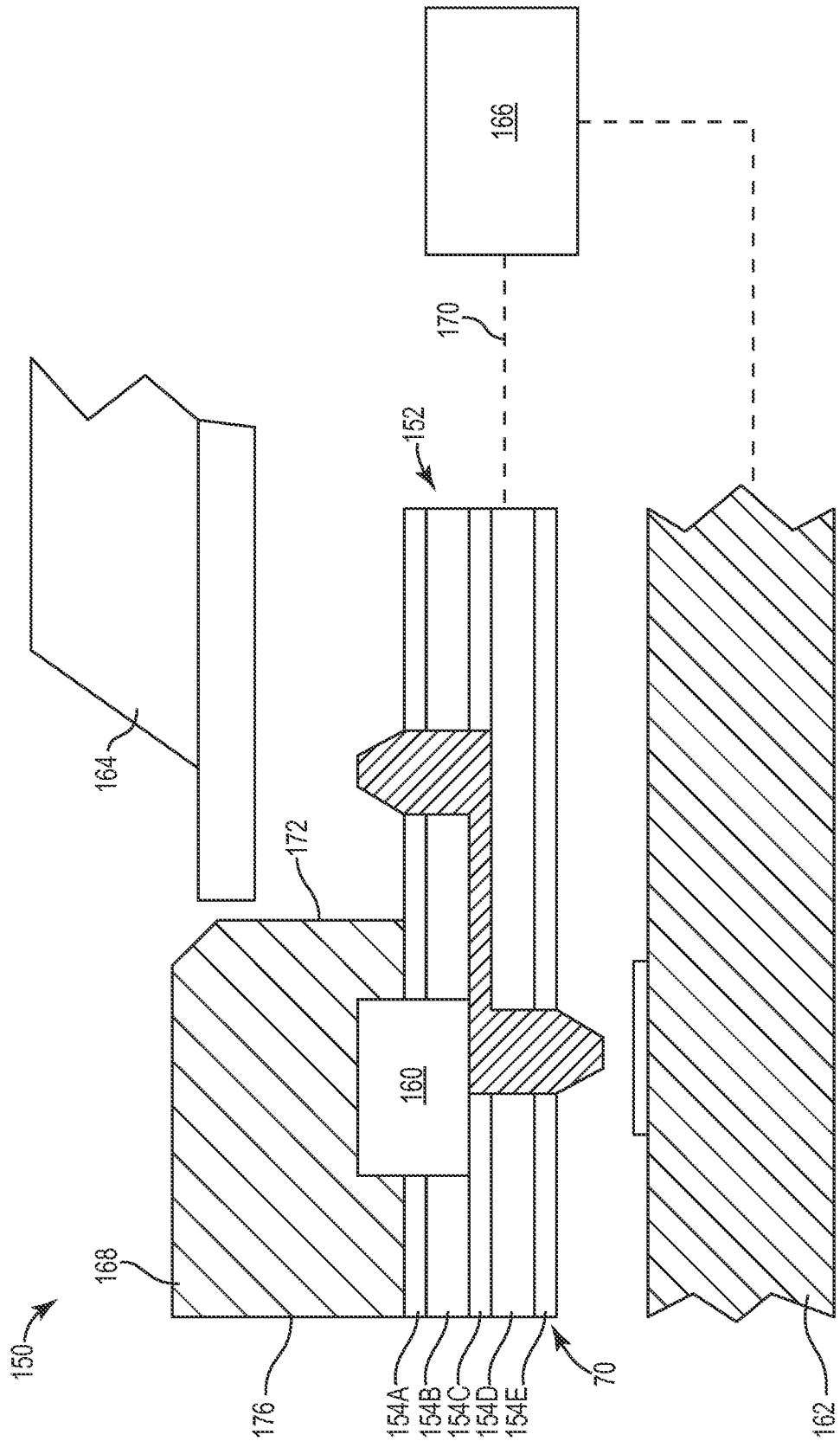
166
170
152
164
172
160
168
150
176
154A
154B
154C
154D
154E
70
162

Fig. 7

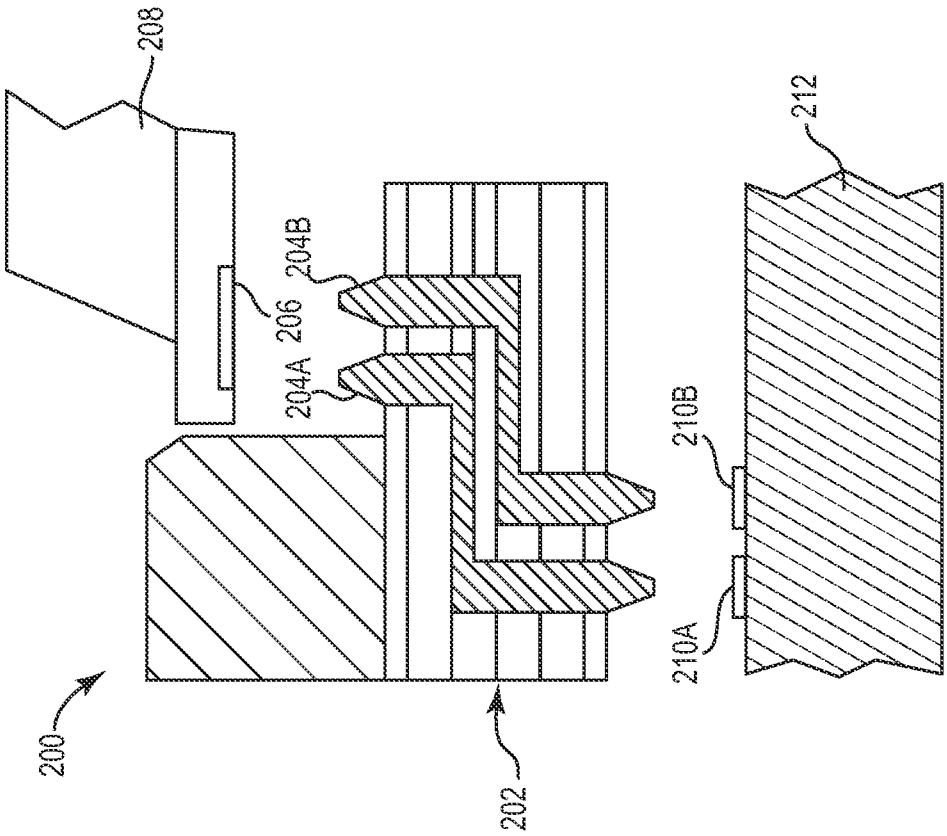

Fig. 8

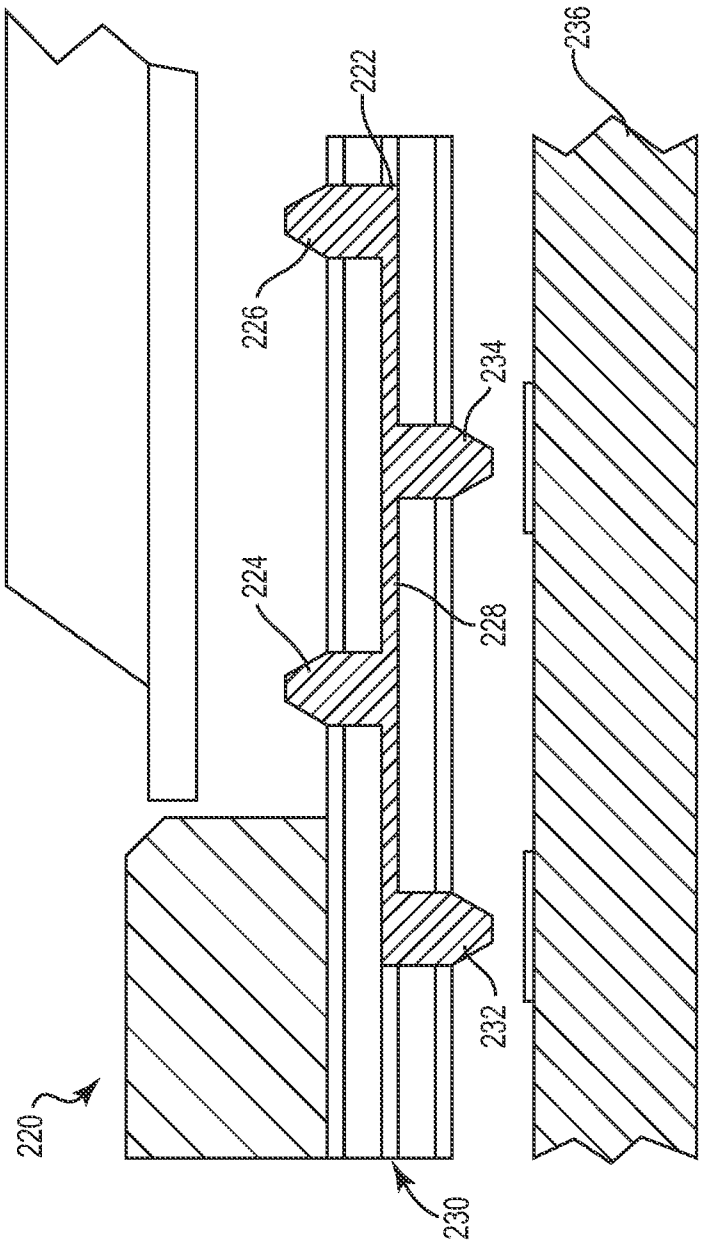

Fig. 9

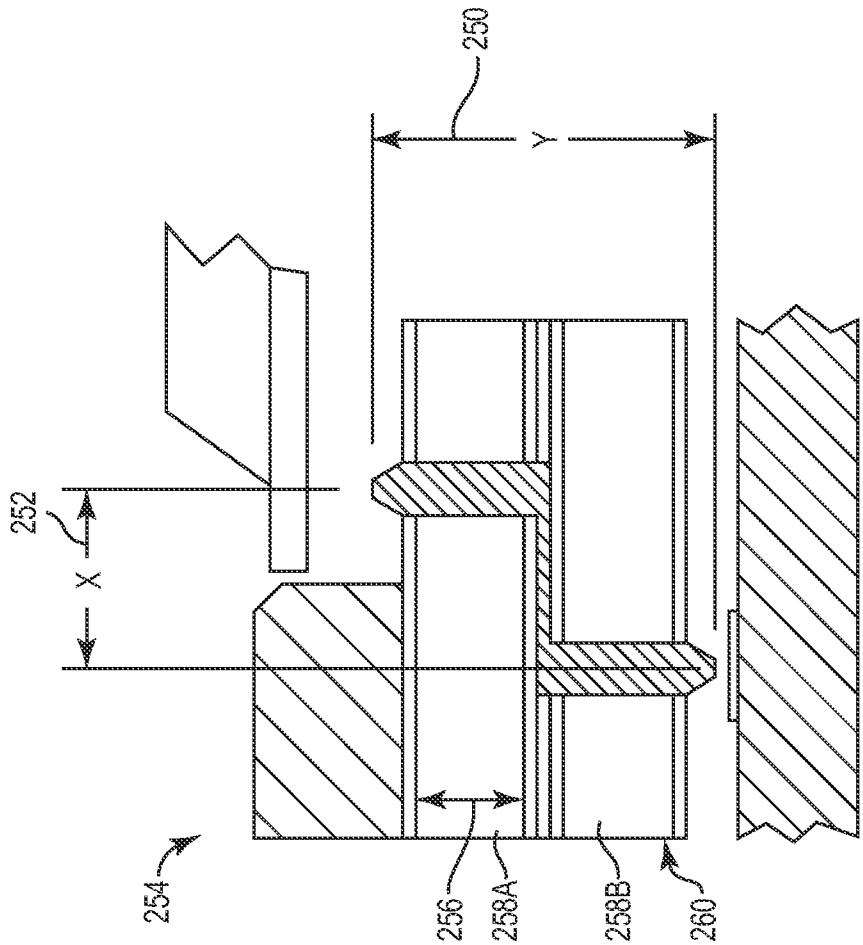

Fig. 10

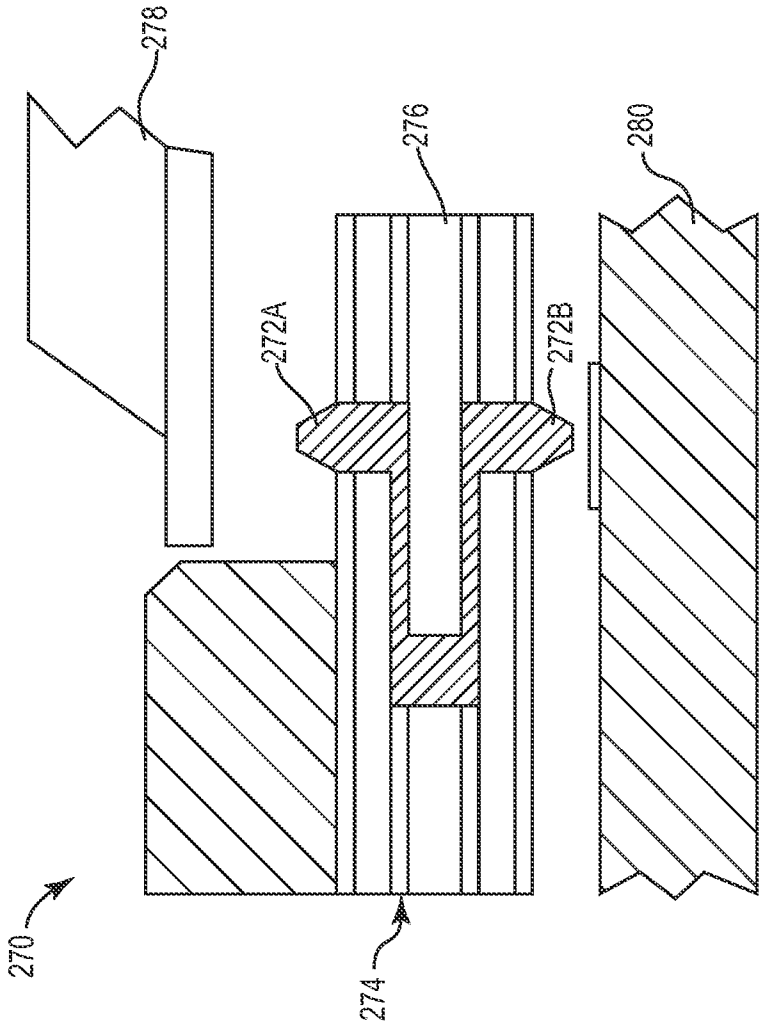

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 10/36397

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01R 12/00 (2010.01)
USPC - 439/68
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 439/55

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
PubWEST (PGPB, USPT, EPAB, JPAB); Google
Search terms: IC, PCB, test, plug, bread, board, panel, socket, recess, multi, plural, several, may, trace, layer, connect, interconnect, pa

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (PGPB, USPT, EPAB, JPAB); Google
Search terms: IC, PCB, test, plug, bread, board, panel, socket, recess, multi, plural, several, may, trace, layer, connect, interconnect, pad, contact, et al.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2006/0160379 A1 (Rathbum) 20 July 2006 (20.07.2006), para [0018]-[0129], Fig 1-20	1-17, 22-34 ---------- 18-21, 35-39
Y	US 2004/0243348 A1 (Minatani) 02 December 2004 (02.12.2004), para [0026]-[0062]	18-21, 35-39
A	US 2001/0012707 A1 (Ho et al.) 09 August 2001 (09.08.2001), entire document	1-39
A	US 2003/0162418 A1 (Yamada) 28 August 2003 (28.08.2003), entire document	1-39

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 July 2010 (15.07.2010)	27 JUL 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774