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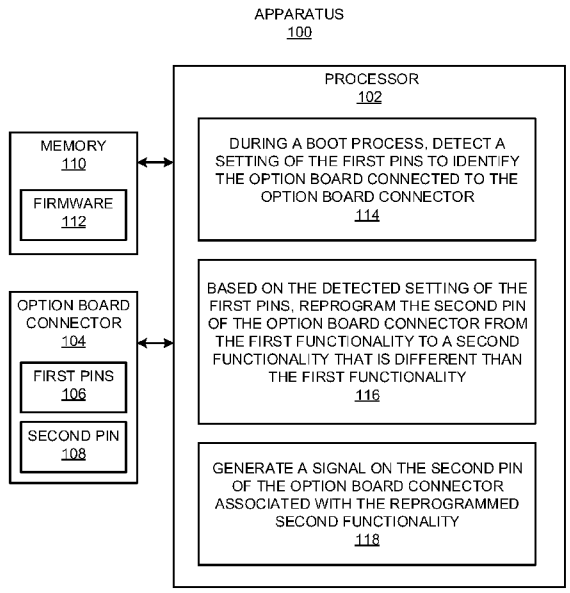

FIG. 1

(57) Abstract: According to examples, an apparatus may include an option board connector having a plurality of first pins that identify an option board to be coupled to the option board connector and a second pin that is programmed for a first functionality, a memory storing a firmware, and a processor. In some examples, the processor may detect a setting of the plurality of first pins to identify the option board connected to the option board connector during a boot process. Based on the detected setting of the plurality of first pins, the processor may reprogram the second pin of the option board connector from the first functionality to a second functionality that is different than the first functionality. The processor may generate a signal on the second pin of the option board connector associated with the reprogrammed second functionality.

REPROGRAM A PIN OF AN OPTION BOARD CONNECTOR

BACKGROUND

[0001] Electronic apparatuses, such as computing devices, may be implemented to perform various functions. The electronic apparatuses may support option boards that enable additional functions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Features of the present disclosure are illustrated by way of example and not limited in the following figure(s), in which like numerals indicate like elements, in which:

[0003] FIG. 1 shows a block diagram of an example apparatus that may detect a setting of a plurality of first pins to identify an option board connected to an option board connector and reprogram a second pin of the option board connector based on the detected setting of the plurality of first pins;

[0004] FIG. 2 shows a block diagram of an example system in which the example apparatus depicted in FIG. 1 may be implemented;

[0005] FIG 3A shows a block diagram of an example controller and an example option board connector, as depicted in FIGS. 1 and 2, having a reprogrammable pin;

[0006] FIG 3B shows a block diagram of an example option board, as depicted in FIGS. 1 and 2, having a pin associated with the reprogrammable pin of the example option board connector depicted in FIG. 3A;

[0007] FIG. 4 shows a flow diagram of an example method for reprogramming a pin on an option board connector based on an identification of the option board connected to the option board connector; and

[0008] FIG. 5 shows a block diagram of an example non-transitory

computer-readable medium that may have stored thereon computer-readable instructions to reprogram a pin on an option board connector based on an identification of the option board connected to the option board connector.

DETAILED DESCRIPTION

[0009] For simplicity and illustrative purposes, the present disclosure is described by referring mainly to examples. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be readily apparent, however, that the present disclosure may be practiced without limitation to these specific details. In other instances, some methods and structures have not been described in detail so as not to unnecessarily obscure the present disclosure.

[0010] Throughout the present disclosure, the terms “a” and “an” are intended to denote at least one of a particular element. As used herein, the term “includes” means includes but not limited to, the term “including” means including but not limited to. The term “based on” means based at least in part on.

[0011] Disclosed herein are apparatuses, methods, and computer-readable mediums to reprogram a pin of an option board connector disposed in an electronic device. Generally, electronic devices, such as computers, laptops, thin clients, or the like, may be set up to accommodate various functions. In some examples, the electronic devices may support option boards (also referred to herein as option cards), connected to option board connectors, to provide additional functionality to the electronic devices. In some examples, the electronic devices may reprogram certain option board connector pins, so that the option board connector may accommodate a greater number and types of option boards. For instance, the option board connector may be initially implemented to not include pins for certain signal types, such as general-purpose input/output (GPIO) pins. In some examples, the electronic devices may repurpose some unused pins on the option board connector by reprogramming the pins to support a desired signal type for a particular type of option board that is installed.

[0012] In some examples, an apparatus may include an option board connector, a memory storing a firmware, and a processor. The option board connector may include a plurality of first pins that may identify an option board to be coupled to the option board connector and a second pin that may be programmed for a first functionality. During a boot process, the processor may detect a setting of the plurality of first pins to identify the option board connected to the option board connector. Based on the detected setting of the plurality of first pins, the processor may reprogram the second pin of the option board connector from the first functionality to a second functionality that is different than the first functionality. In some examples, the processor may reprogram a plurality of second pins based on the detected setting of the plurality of first pins. Once the relevant pin(s) on the controller 104 has been reprogrammed, the processor may generate a signal on the second pin(s) of the option board connector associated with the reprogrammed second functionality.

[0013] Through implementation of the features of the present disclosure, option board connector pins may be repurposed, thereby enabling the option board connector to support signals not originally defined when the option board connector was conceived. In some examples, GPIO signals may be created from unused serial port signals to support a new option board not originally defined for in the option board connector. By repurposing unused pins, the option board connector may have a reduced pin count since not all pins may need to be defined, and the option board connector may support a greater number of functionalities with fewer pins. Additionally, a new option board may be implemented even when a new functionality may be implemented and the pins were not previously defined in the original conception of the option board connector.

[0014] Reference is made to FIGS. 1 and 2. FIG. 1 shows a block diagram of an example apparatus 100 that may detect a setting of a plurality of first pins 106 to identify an option board connected to an option board connector 104 and reprogram a second pin 108 of the option board connector 104 based on the detected setting of the plurality of first pins 106. FIG. 2 shows a block diagram of an example system 200 in which the example apparatus 100 depicted in FIG. 1

may be implemented. It should be understood that the example apparatus 100 depicted in FIG. 1 and the example system 200 depicted in FIG. 2 may include additional features and that some of the features described herein may be removed and/or modified without departing from the scopes of the apparatus 100 and/or the system 200.

[0015] The apparatus 100 and the system 200 may each be a personal computer, a laptop computer, a tablet computer, a smartphone, a two-dimensional printer, a three-dimensional printer, a server, a node in a network (such as a data center), a thin client, a network gateway, a network router, an electronic device such as Internet of Things (IoT) device, a robotic device, and/or the like. As shown, the apparatus 100 may include a processor 102 and a non-transitory computer-readable medium, e.g., a memory 110. The processor 102 may be a semiconductor-based microprocessor, a central processing unit (CPU), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), and/or other hardware device. Although the apparatus 100 is depicted as having a single processor 102, it should be understood that the apparatus 100 may include additional processors and/or cores without departing from a scope of the apparatus 100. In this regard, references to a single processor 102 as well as to a single memory 110 may be understood to pertain to multiple processors 102 and/or multiple memories 110.

[0016] The processor 102 may include a controller 202 integrated into the processor 102. In some examples, the controller 202 may be a multiplexer, a super I/O chip, or the like. Although the controller 202 is depicted in FIG. 2 as being integrated into the processor 102, the controller 202 may alternatively be separate from the controller 202 in some examples. In these examples, the controller 202 may be connected to the processor 102 and the option board connector 104.

[0017] The memory 110 may be an electronic, magnetic, optical, or other physical storage device that contains or stores executable instructions. The memory 110 may be, for example, Read-Only Memory (ROM), flash memory, solid state drive, Random Access memory (RAM), an Electrically Erasable

Programmable Read-Only Memory (EEPROM), a storage device, an optical disc, or the like. The memory 110 may be a non-transitory computer-readable medium. The term "non-transitory" does not encompass transitory propagating signals. In some examples and as shown in FIG. 1, the memory 110 may have stored thereon a firmware 112. The firmware 112 may generally be defined as a set of instructions that may provide control for hardware in and/or attached to the apparatus 100. In some instances, the firmware 112 may provide a standardized operating environment for more complicated software, such as an operating system, in the apparatus 100 or may act as an operating system for the apparatus 100. According to examples, the firmware 112 may be a Unified Extensible Firmware Interface (UEFI) or a Basic Input/Output System (BIOS). In these examples, the firmware 112 may be termed "bootup firmware".

[0018] In examples in which the firmware 112 is a UEFI or a BIOS, the firmware 112 may ensure that all of the components in and/or connected to the apparatus 100 are functional. Particularly, the firmware 112 may be responsible for establishing the association between components (e.g., disk drives, video controllers, keyboard, mouse, etc.) and the operating system that the apparatus 100 executes. In some examples where some components are connected through the option board connector 104, the firmware 112 may reprogram the option board connector 104 during the boot process. The firmware 112 may also include data and instructions that may enable the operating system to access hardware of the apparatus 100. In addition, during the apparatus 100 bootup, the firmware 112 may first perform a Power-On Self-Test (POST) and may then proceed to load the operating system.

[0019] The option board connector 104 may include a plurality of pins to connect to various types of option boards, such as an option board 204 depicted in FIG. 2. The plurality of pins of the option board connector 104 may include a plurality of first pins 106 and a second pin 108. The plurality of first pins 106 may be used to detect the installed option board, and the second pin 108 may be programmed for various functions of the option board, as will be described in further detail hereinafter.

[0020] As shown in FIG. 1, the processor 102 may perform various operations 114-118 to reprogram a pin on an option board connector 104 to have a different functionality, in order to repurpose the pin for use for the different functionality. The operations 114-118 may be computer-readable instructions, e.g., non-transitory computer-readable instructions. In other examples, the apparatus 100 may include hardware logic blocks or a combination of instructions and hardware logic blocks to implement or execute functions corresponding to the operations 114-118. As used herein, hardware logic blocks may be configurable logic blocks of an FPGA.

[0021] The processor 102 may execute the operation 114 to detect a setting of the plurality of first pins 106 to identify the option board 204 connected to the option board connector 104. The processor 102 identify the option board 204 during a boot process. In some examples, the option board connector 104 may include a plurality of pins to allow for various types of option boards 204 to be connected to the apparatus 100. Among the plurality of pins, the plurality of first pins 106 may be disposed on the option board connector 104 to identify the option board 204 that is connected to the apparatus 100. By way of particular example, the setting of the plurality of first pins 106 may identify the option board 204 connected to the option board connector 104 as being one of an Ethernet board, a universal serial bus (USB) options board, a serial port board, a video option board, or the like.

[0022] In some examples, the memory 110 may store option board information 206 related to different types of option boards 204 that the apparatus 100 may support. The option board information 206 may include information such as identification information for different option boards 204, the first pin functionality 208 and the second pin functionality 210 of the option boards 204, information for reprogramming the second pin 108 or a group of the second pins 108, or the like.

[0023] In some examples, the option board information 206 may include a lookup table of different settings of the plurality of first pins 106 and a corresponding option board 204 and associated first and second pin

functionalities 208 and 210. For instance, the processor 102 may identify, based on the detected setting of the plurality of first pins 106, the option board 204 that is mounted to the option board connector 104.

[0024] The processor 102 may execute the operation 116 to, based on the detected setting of the plurality of first pins 106, reprogram the second pin 108 of the option board connector 104 from a first functionality 208 to a second functionality 210 that is different than the first functionality 208.

[0025] Not all option boards 204 may use all signals present on the option board connector 104. In some instances, the available pins on the option board connector 104 may not include a pin having a certain type of functionality (e.g., a GPIO pin) that may be used on a particular option board. In some examples, a signal on an unused pin may be reprogrammed so that the pin may be repurposed for a certain missing type of pin for a particular option board. By way of particular example, the second pin 108 on the option board connector 104 may be implemented to initially have a first functionality 208, such as a serial port signal. In some instances, a mounted option board 204 may not need the first functionality 208. In this case, the processor 102 may reprogram the unused second pin 108 to the second functionality 210 based on the identification of the connected option board 204.

[0026] By way of particular example and for purposes of illustration, the plurality of first pins 106 may be a group of three pins, and the option board 204 identified by the plurality of first pins may be an Ethernet board. During the boot process, the processor 102 may sense signals on the group of three pins to identify the option board 204 that is coupled to the option board connector 104. For instance, a combination of 0 0 1 respectively on the three pins may be associated with an Ethernet board, and a combination of 1 1 1 may indicate that no option board is connected.

[0027] In some examples, the Ethernet board may include an Ethernet circuit and a power circuit. The Ethernet board may be implemented to meet certain energy regulations by controlling power to the Ethernet circuit when not in use. In this instance, a GPIO signal from a controller, such as the controller 202

as depicted in FIG. 2, may be used to turn the power to the Ethernet circuit on or off. By way of particular example, the processor 102 may determine that an unused second pin 108 on the option board connector 104, which may be associated with a first functionality 208, such as a serial port signal and which may be unused in the Ethernet board, may be available. The processor 102 may determine that the second pin 108 is coupled to a pin on the controller 202 that is reprogrammable. Based on the option board information 206 stored in the memory 110, for instance, the processor 102 may reprogram the second pin 108 from the first functionality 208 to the second functionality 210. Continuing with the example of the Ethernet board, the processor 102 may reprogram the second pin 108 from a serial port signal to a GPIO signal that may turn on/off the power to the Ethernet circuit.

[0028] In some examples, the controller 202 may be disposed on a motherboard and may be integrated with the processor 102, as depicted in FIG. 2. As another example, the controller 202 may be disposed separately from the processor 102. By way of particular examples, the controller 202 on the motherboard may be a multiplexer, a super input/output (I/O) chip, or the like. When the second pin 108 is coupled to a reconfigurable output pin on a controller 202, such as a super I/O chip as depicted in FIG. 3A, the processor 102 may cause the controller 202 to reprogram the second pin 108, such as from a serial port pin to the GPIO pin.

[0029] The processor 102 may execute the operation 118 to generate a signal on the second pin 108 of the option board connector 104 associated with the reprogrammed second functionality 210. Continuing with the example in which the option board 204 is identified as the Ethernet board, the processor 102 may generate a power-enable signal to the power circuit to power on/off the Ethernet circuit. In some examples, the processor 102 may instruct the controller 202 to reprogram the second pin 108 to be a power-enable signal pin and the controller 202 may generate the power-enable signal on the reprogrammed power-enable signal pin.

[0030] Reference is now made to FIGS. 3A and 3B. FIG. 3A shows a block

diagram of an example controller 202 and an example option board connector 104, as depicted in FIGS. 1 and 2, having a reprogrammable pin 108-1. FIG. 3B shows a block diagram of an example option board 204, as depicted in FIGS. 1 and 2, having a second pin 304-1 associated with the reprogrammable pin 108-1 of the example option board connector 104 depicted in FIG. 3A. It should be understood that the example option board connector 104 and controller 202 depicted in FIG. 3A and the example option board 204 depicted in FIG. 3B may include additional features and that some of the features described herein may be removed and/or modified without departing from the scope of the option board connector 104/controller 202 and the option board 204. The descriptions of FIGS. 3A and 3B are made with reference to the features shown in FIGS. 1 and 2.

[0031] As shown in FIG. 3A, the option board connector 104 may include a plurality of pins, including a plurality of first pins 106-1 to 106-n, in which the variable "n" may represent a value greater than one, and a plurality of second pins 108-1 to 108-p, in which the variable "p" may represent a value greater than one. The plurality of first pins 106-1 to 106-n may be a predetermined group of pins used to identify the option board 204 mounted on the option board connector 104. The number of first pins 106-1 to 106-n may be varied based on a number of different option boards 204 that the option board connector 104 may support. By way of particular example, if the number of first pins 106-1 to 106-n is three, the settings available on the plurality of first pins 106-1 to 106-n may identify up to 8 option boards 204. While the option board connector 104 has been described as including a plurality of first pins 106-1 to 106-n, it should be understood that the option board connector 104 may include a single first pin 106-1 used to identify the option board 204 mounted on the option board connector 104.

[0032] The second pins 108-1 to 108-p may be pins that are coupled to a controller 202 and designated for predetermined functions. The second pins 108-1 to 108-p may be connected to respective pins on the controller 202. In some examples, one of the second pins 108-1 to 108-p or multiple ones of the second pins 108-1 to 108-p may be unused and may be reprogrammable at the controller 202.

[0033] By way of particular example, the processor 102 may reprogram an unused one of the second pins 108-1 to 108-p based on an identification of the option board 204 using the plurality of first pins 106-1 to 106-n. For instance, the processor 102 may cause a super I/O chip (the controller 202) connected to the option board connector 104 to reprogram the pin corresponding to a particular second pin, such as reprogrammable pin 108-1. By way of example, the super I/O chip may reprogram a serial port pin to a GPIO pin.

[0034] By way of particular example and for illustrative purposes, the option board 204 may be an Ethernet board as shown in FIG. 3B. In this instance, the option board 204 may include the plurality of first pins 302-1 to 302-n used to identify the option board 204 as an Ethernet board and second pins 304-1 to 304-m to receive signals from the controller 202 to operate the Ethernet board. The plurality of first pins 302-1 to 302-n may correspond to the plurality of first pins 106-1 to 106-n of the option board connector 104. In this example, a second pin 304-1 on the Ethernet board 204 may be a power-enable serial pin to turn on/off power to the Ethernet board. Based on an identification of the Ethernet board 204 at the option board connector 104, the processor 102 may reprogram an unused one of the second pins 108-1-108-p on the option board connector 104, such as a second pin 108-1, to support the power-enable serial pin on the Ethernet board 204, such as the second pin 304-1. For instance, the signal on the reprogrammed pin 108-1 on the option board connector 104 may be a GPIO signal from the super I/O chip (the controller 202) that may be reprogrammed to control power to a circuit on the Ethernet board.

[0035] Various manners in which the processor 102 may operate are discussed in greater detail with respect to the method 400 depicted in FIG. 4. Particularly, FIG. 4 depicts a flow diagram of an example method 400 for reprogramming a pin on an option board connector based on an identification of the option board connected to the option board connector. It should be understood that the method 400 depicted in FIG. 4 may include additional operations and that some of the operations described therein may be removed and/or modified without departing from the scopes of the method 400. The description of the method 400 is made with reference to the features depicted in

FIGS. 1 to 3B for purposes of illustration.

[0036] At block 402, the processor 102 may identify an option board 204 connected to an option board connector 104. The processor 102 may identify the option board 204 during a boot process, such during Power-On Self-Test (POST). In some examples, the processor 102 may identify a type of the option board 204 connected to the option board connector 104 during POST. The type of the option board 204 may be identified based on a detected setting of a predetermined group of pins on the option board connector 104, such as the first pins 106 depicted in FIG. 1.

[0037] At block 404, the processor 102 may, based on an identification of the option board 204, reprogram a second pin 108-1 on the option board connector 104 from a serial port pin to a GPIO pin. In some examples, the second pin 108-1 on the option board connector 104 may be coupled to a predetermined output on a controller, such as the controller 202 depicted in FIGS. 2 and 3A. In some instances, the controller 202 may be a super I/O chip and the processor 102 may reprogram the predetermined output on the super I/O chip from a serial port type output to a GPIO type output.

[0038] At block 406, the processor 102 may complete the boot process to boot up with the option board connector 104 including the reprogrammed pin 108-1. In some examples, the processor 102 may generate the GPIO type output on the reprogrammed pin 108-1 to control the option board 204. By way of particular example, in case the option board 204 is an Ethernet board, the reprogrammed pin 108-1 may be repurposed as a GPIO pin connected to a reprogrammed pin on the super I/O chip to generate a power-enable signal for the Ethernet board.

[0039] Some or all of the operations set forth in the method 400 may be included as utilities, programs, or subprograms, in any desired computer accessible medium. In addition, the method 400 may be embodied by computer programs, which may exist in a variety of forms both active and inactive. For example, they may exist as computer-readable instructions, including source code, object code, executable code or other formats. Any of the above may be embodied on a non-transitory computer-readable storage medium.

[0040] Examples of non-transitory computer-readable storage media include computer system RAM, ROM, EPROM, EEPROM, and magnetic or optical disks or tapes. It is therefore to be understood that any electronic device capable of executing the above-described functions may perform those functions enumerated above.

[0041] Turning now to FIG. 5, there is shown a block diagram of a non-transitory computer-readable medium 500 that may have stored thereon computer-readable instructions to reprogram a pin on an option board connector based on an identification of the option board connected to the option board connector. It should be understood that the computer-readable medium 500 depicted in FIG. 5 may include additional instructions and that some of the instructions described herein may be removed and/or modified without departing from the scope of the computer-readable medium 500 disclosed herein. The computer-readable medium 500 may be a non-transitory computer-readable medium. The term “non-transitory” does not encompass transitory propagating signals.

[0042] The computer-readable medium 500 may have stored thereon computer-readable instructions 502-508 that a processor, such as the processor 102 depicted in FIGS. 1-2, may execute. The computer-readable medium 500 may be an electronic, magnetic, optical, or other physical storage device that contains or stores executable instructions. The computer-readable medium 500 may be, for example, RAM, EEPROM, a storage device, an optical disc, and the like.

[0043] The processor may fetch, decode, and execute the instructions 502 to detect a setting of the plurality of first pins, such as the plurality of first pins 106 depicted in FIG. 1, on an option board connector, such as the option board connector 104 depicted in FIGS. 1 to 3A, during a boot process. In some examples, the plurality of first pins 106 may be a predetermined number of designated pins, such as the first pins 106-1 to 106-n depicted in FIG. 3A, disposed on the option board connector 104. The designated first pins 106-1 to 106-n on the option board connector 104 may be coupled to corresponding pins

on the option board 204, such as first pins 302-1 to 302-n as depicted in FIG. 3B, to identify the option board 204.

[0044] The processor may fetch, decode, and execute the instructions 504 to identify a type of an option board 204 connected to the option board connector 104 based on the detected setting of the plurality of first pins 106. By way of particular example, the option board 204 may be one of an Ethernet board, a USB options board, a serial port board, a video option board, or the like. The plurality of first pins 106 may include a predetermined number of pins for identifying the type of the option board 204.

[0045] The processor may fetch, decode, and execute the instructions 506 to, based on the identified type of the option board 204, reprogram a second pin 108 on the option board connector 104 from a first functionality 208 to a second functionality 210 that is different than the first functionality 208.

[0046] The processor may fetch, decode, and execute the instructions 508 to complete the boot process to boot up with the option board connector including the second functionality for the second pin of the option board connector.

[0047] In some examples, the processor 102 may reprogram the second pin 108 to be a GPIO pin. The second pin 108 may be coupled to a predetermined output on controller 202, such as a super I/O chip depicted in FIG. 3A, and the processor 102 may cause the super I/O chip to reprogram the predetermined output from a serial port output to a GPIO output.

[0048] In some examples, the processor 102 may identify the type of the option board connected to the option board connector 104, for instance, as an Ethernet board, a USB options board, a serial port board, or a video option board. By way of particular example, the processor 102 may identify, based on the detected setting of the plurality of first pins 106, the type of the option board 204 connected to the option board connector 104 as being an Ethernet board. In some examples, the Ethernet board may include an Ethernet circuit and a power circuit. For instance, the processor 102 may reprogram the second pin 108 on the option board connector 104 to be a power-enable signal pin. In this instance, the processor 102 may send a power-enable signal to the power circuit through the

power-enable signal pin to power on/off the Ethernet circuit.

[0049] What has been described and illustrated herein is an example of the disclosure along with some of its variations. The terms, descriptions and figures used herein are set forth by way of illustration and are not meant as limitations. Many variations are possible within the spirit and scope of the disclosure, which is intended to be defined by the following claims -- and their equivalents -- in which all terms are meant in their broadest reasonable sense unless otherwise indicated.

What is claimed is:

1. An apparatus comprising:

an option board connector having a plurality of first pins that identify an option board to be coupled to the option board connector and a second pin that is programmed for a first functionality;

a memory storing a firmware; and

a processor to:

during a boot process, detect a setting of the plurality of first pins to identify the option board connected to the option board connector;

based on the detected setting of the plurality of first pins, reprogram the second pin of the option board connector from the first functionality to a second functionality that is different than the first functionality; and

generate a signal on the second pin of the option board connector associated with the reprogrammed second functionality.

2. The apparatus of claim 1, wherein, based on the detected setting of the plurality of first pins, the processor is to reprogram the second pin to be a general-purpose input/output (GPIO) pin.

3. The apparatus of claim 2, wherein the second pin is coupled to a predetermined output on a super I/O chip, and the processor is to cause the super I/O chip to reprogram the second pin from a serial port pin to the GPIO pin.

4. The apparatus of claim 1, wherein the second pin is coupled to a controller on a motherboard, and based on the detected setting of the plurality of first pins to identify the option board connected to the option board connector, the processor is to cause the controller on the motherboard to reprogram the second pin to be a general-purpose input/output (GPIO) pin.

5. The apparatus of claim 4, wherein the controller on the motherboard is a multiplexer and/or a super I/O chip.

6. The apparatus of claim 1, wherein the setting of the plurality of first pins identifies the option board connected to the option board connector as being one of an Ethernet board, a universal serial bus (USB) options board, a serial port board, or a video option board.

7. The apparatus of claim 1, wherein the setting of the plurality of first pins identifies the option board connected to the option board connector as being an Ethernet board, the Ethernet board having an Ethernet circuit and a power circuit.

8. The apparatus of claim 7, wherein the processor is to reprogram the second pin on the option board connector to be a power-enable signal pin, the power-enable signal pin to send a power-enable signal to the power circuit to power on/off the Ethernet circuit.

9. A method comprising:

during a boot process, identifying, by a processor, an option board connected to an option board connector;

based on an identification of the option board, reprogramming, by the processor, a pin on the option board connector from a serial port pin to a general-purpose input/output (GPIO) pin; and

completing, by the processor, the boot process to boot up with the option board connector including the reprogrammed pin.

10. The method of claim 9, wherein the pin on the option board connector is coupled to a predetermined output on a super I/O chip, the method further comprising:

reprogramming, by the super I/O chip, the predetermined output on the super I/O chip from a serial port type output to a GPIO type output; and

generating the GPIO type output on the reprogrammed pin to control the option board.

11. The method of claim 9, further comprising:

initiating a power-on self-test (POST) during the boot process; and

identifying a type of the option board connected to the option board connector during the POST, the type of the option board being identified based on a detected setting of a predetermined group of pins on the option board connector.

12. A non-transitory computer-readable medium on which is stored computer-readable instructions that when executed by a processor, cause the processor to:

during a boot process, detect a setting of a plurality of first pins on an option board connector;

identify a type of an option board connected to the option board connector based on the detected setting of the plurality of first pins;

based on the identified type of the option board, reprogram a second pin on the option board connector from a first functionality to a second functionality that is different than the first functionality; and

complete the boot process to boot up with the option board connector including the second functionality for the second pin of the option board connector.

13. The non-transitory computer-readable medium of claim 12, wherein, based on the detected setting of the plurality of first pins, the instructions further cause the processor to:

reprogram the second pin to be a general-purpose input/output (GPIO) pin,

wherein the second pin is coupled to a predetermined output on a super input/output (I/O) chip and the processor causes the super I/O chip to reprogram the predetermined output from a serial port output to a GPIO output.

14. The non-transitory computer-readable medium of claim 12, wherein the instructions further cause the processor to:

identify the type of the option board connected to the option board connector as being one of an Ethernet board, a universal serial bus (USB) options

board, a serial port board, or a video option board.

15. The non-transitory computer-readable medium of claim 12, wherein the instructions further cause the processor to:

identify, based on the detected setting of the plurality of first pins, the type of the option board connected to the option board connector as being an Ethernet board, the Ethernet board having an Ethernet circuit and a power circuit,

reprogram the second pin on the option board connector to be a power-enable signal pin; and

send a power-enable signal to the power circuit through the power-enable signal pin to power on/off the Ethernet circuit.

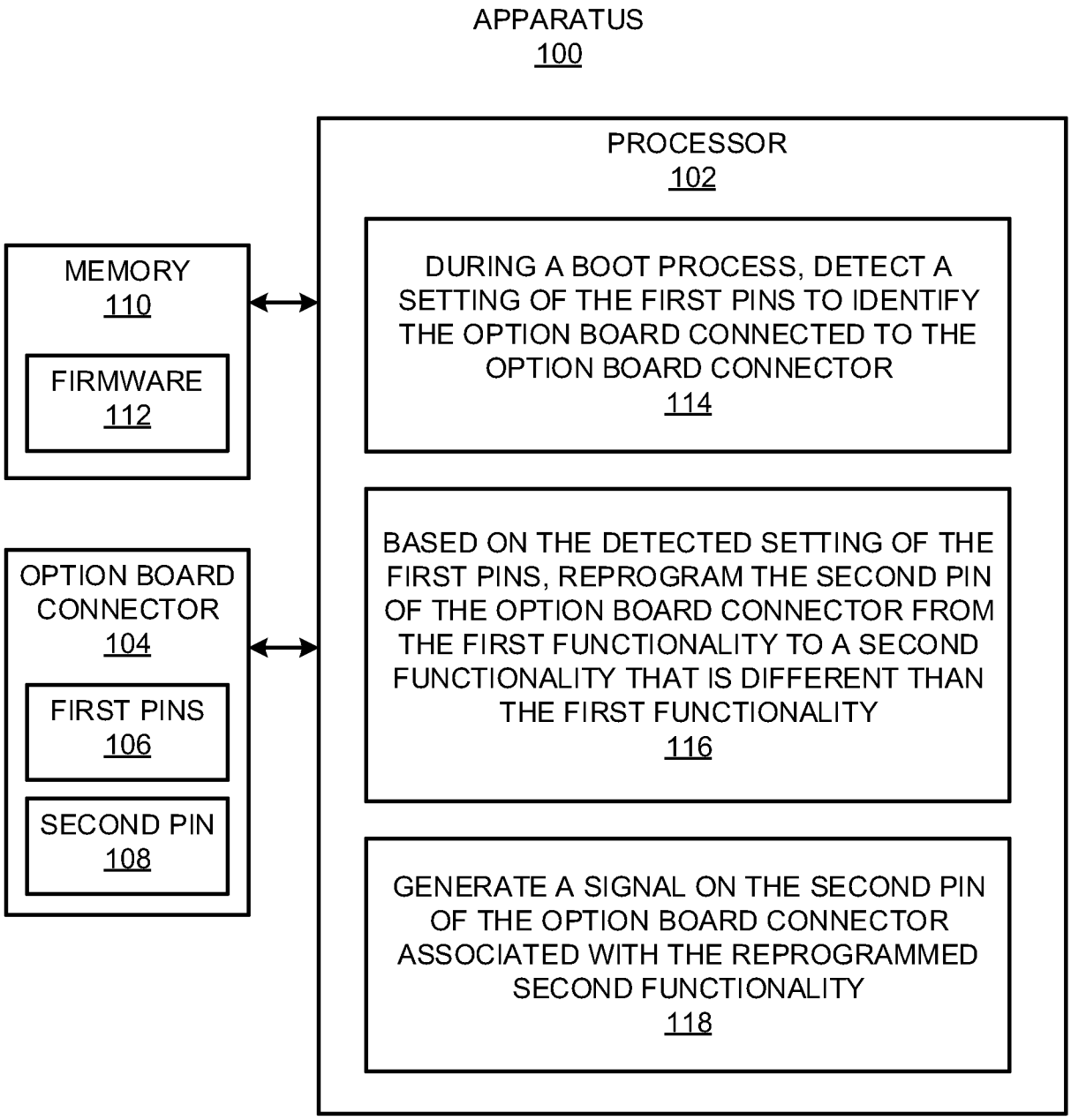
APPARATUS
100
PROCESSOR
102
MEMORY
110
FIRMWARE
112
OPTION BOARD CONNECTOR
104
FIRST PINS
106
SECOND PIN
108
DURING A BOOT PROCESS, DETECT A SETTING OF THE FIRST PINS TO IDENTIFY THE OPTION BOARD CONNECTED TO THE OPTION BOARD CONNECTOR
114
BASED ON THE DETECTED SETTING OF THE FIRST PINS, REPROGRAM THE SECOND PIN OF THE OPTION BOARD CONNECTOR FROM THE FIRST FUNCTIONALITY TO A SECOND FUNCTIONALITY THAT IS DIFFERENT THAN THE FIRST FUNCTIONALITY
116
GENERATE A SIGNAL ON THE SECOND PIN OF THE OPTION BOARD CONNECTOR ASSOCIATED WITH THE REPROGRAMMED SECOND FUNCTIONALITY
118

FIG. 1

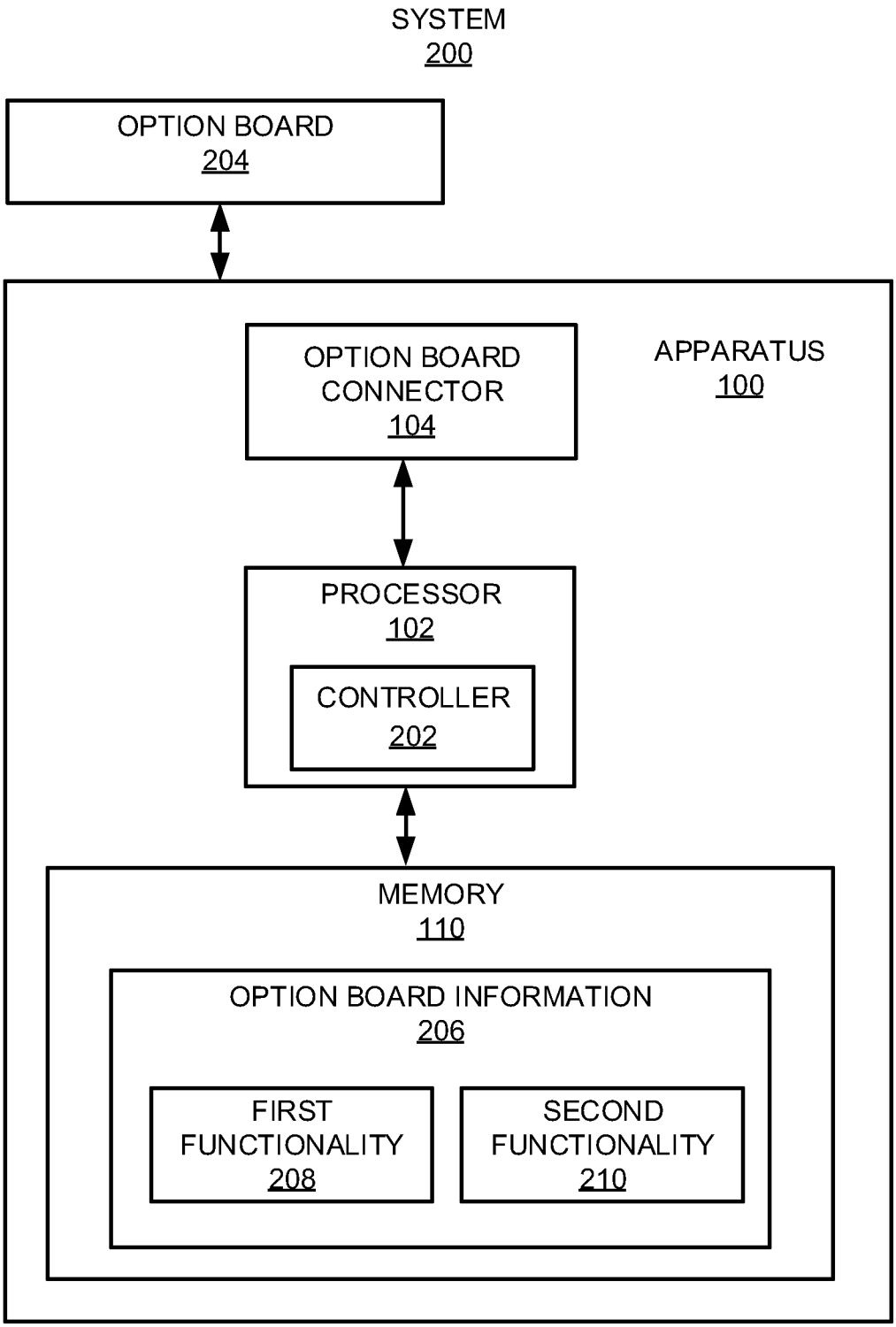
SYSTEM
200
OPTION BOARD
204
APPARATUS
100
OPTION BOARD
CONNECTOR
104
PROCESSOR
102
CONTROLLER
202
MEMORY
110
OPTION BOARD INFORMATION
206
FIRST
FUNCTIONALITY
208
SECOND
FUNCTIONALITY
210

FIG. 2

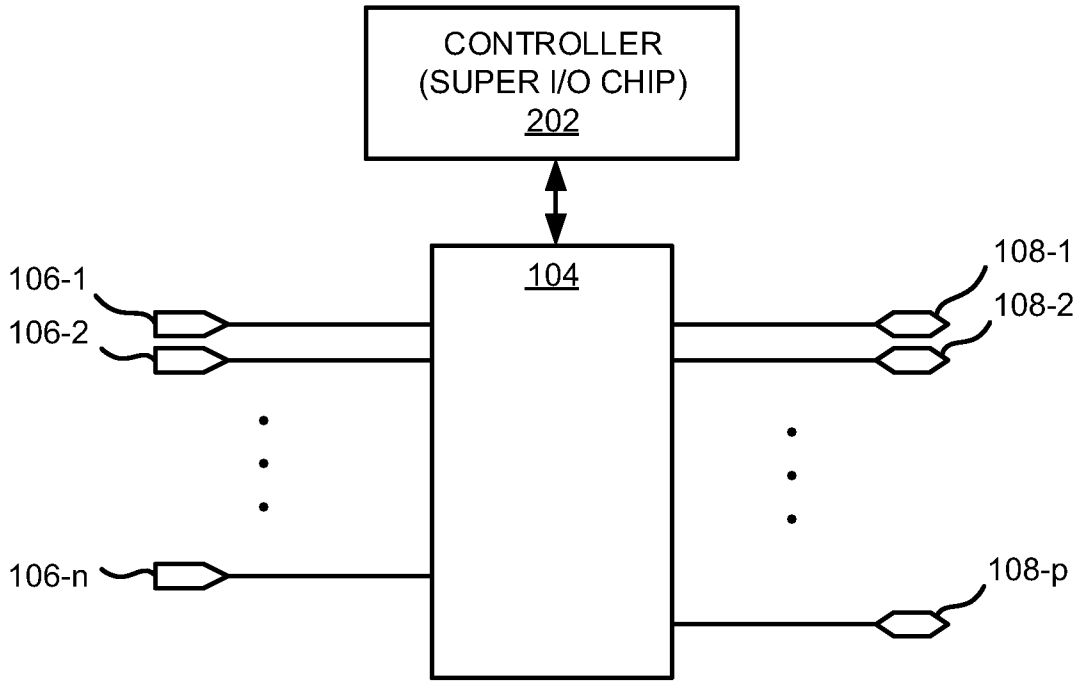
CONTROLLER
(SUPER I/O CHIP)
202
104
106-1
106-2
106-n
108-1
108-2
108-p

FIG. 3A

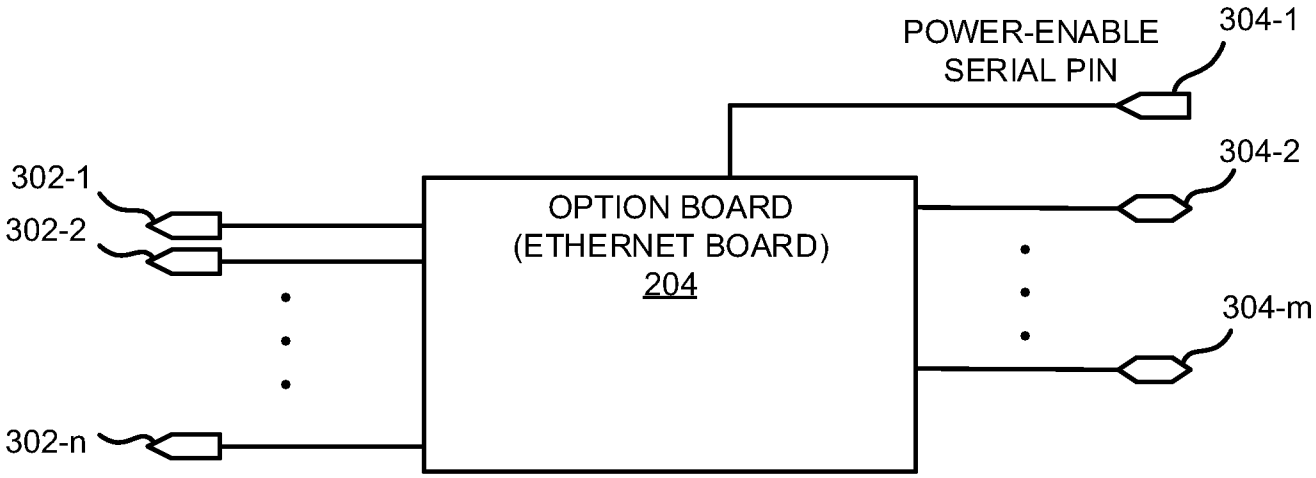
POWER-ENABLE
SERIAL PIN
304-1
304-2
304-m
302-1
302-2
302-n
OPTION BOARD
(ETHERNET BOARD)
204

FIG. 3B

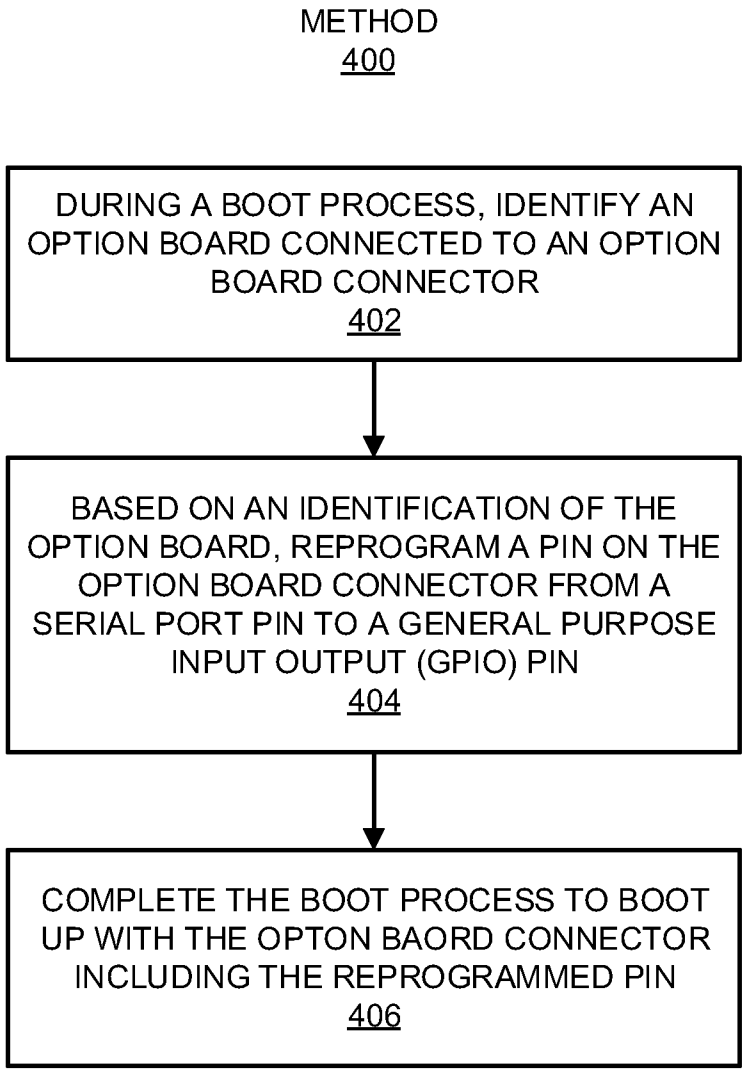
METHOD
400
DURING A BOOT PROCESS, IDENTIFY AN OPTION BOARD CONNECTED TO AN OPTION BOARD CONNECTOR
402
BASED ON AN IDENTIFICATION OF THE OPTION BOARD, REPROGRAM A PIN ON THE OPTION BOARD CONNECTOR FROM A SERIAL PORT PIN TO A GENERAL PURPOSE INPUT OUTPUT (GPIO) PIN
404
COMPLETE THE BOOT PROCESS TO BOOT UP WITH THE OPTON BAORD CONNECTOR INCLUDING THE REPROGRAMMED PIN
406

FIG. 4

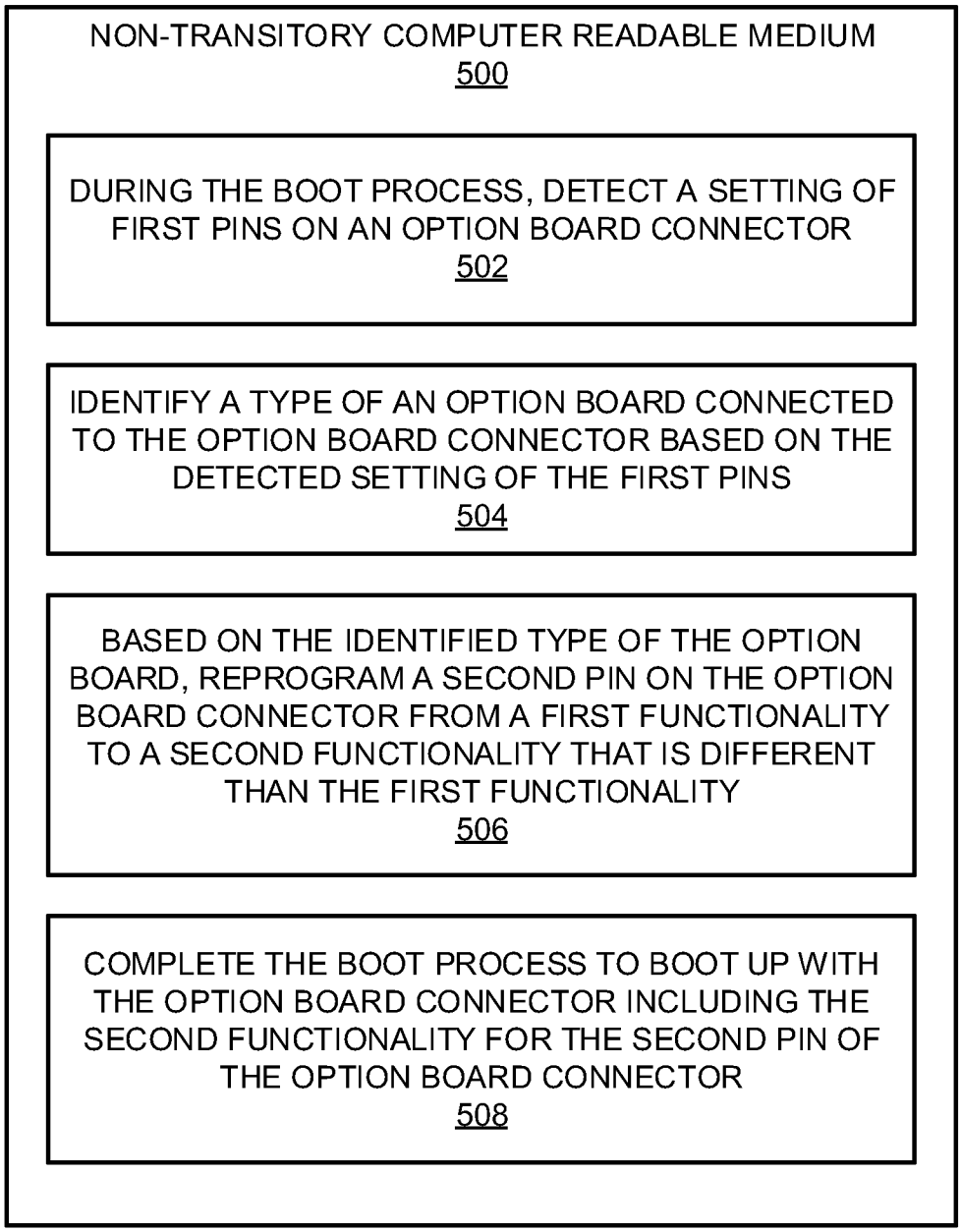
NON-TRANSITORY COMPUTER READABLE MEDIUM
500
DURING THE BOOT PROCESS, DETECT A SETTING OF FIRST PINS ON AN OPTION BOARD CONNECTOR
502
IDENTIFY A TYPE OF AN OPTION BOARD CONNECTED TO THE OPTION BOARD CONNECTOR BASED ON THE DETECTED SETTING OF THE FIRST PINS
504
BASED ON THE IDENTIFIED TYPE OF THE OPTION BOARD, REPROGRAM A SECOND PIN ON THE OPTION BOARD CONNECTOR FROM A FIRST FUNCTIONALITY TO A SECOND FUNCTIONALITY THAT IS DIFFERENT THAN THE FIRST FUNCTIONALITY
506
COMPLETE THE BOOT PROCESS TO BOOT UP WITH THE OPTION BOARD CONNECTOR INCLUDING THE SECOND FUNCTIONALITY FOR THE SECOND PIN OF THE OPTION BOARD CONNECTOR
508

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2020/038734

A. CLASSIFICATION OF SUBJECT MATTER

G05B 15/02 *(2006.01)*
H04L 12/24 *(2006.01)*
H05B 45/35 *(2020.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G05B 15/02, H04L 12/00-12/24, H05B 45/00-45/35

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO Internal), USPTO, PAJ, Espacenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2009/0265792 A1 (RICHARDO L. MARTINEZ et al.) 22.10.2009, abstract, paragraphs [0007], [0015], [0026], claims 12, 22	9 1-8, 10-15
Y	US 8117587 B1 (TESTARDI RICHARD PAUL) 14.02.2012, column 5, line 55-column 6, line 3, column 45, lines 7-11	1-8, 10-15
Y	US 2016/0179744 A1 (ACQIS LLC) 23.06.2016, abstract, paragraphs [0012], [0068], [0074], [0079], [0090], [0106]	5-8, 14, 15
Y	US 2007/0035632 A1 (WILLIAM BRADFORD SILVERNAIL et al.) 15.02.2007, abstract, paragraphs [0189]-[0191]	11

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 December 2020 (29.12.2020)	04 February 2021 (04.02.2021)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer V. Shepelev Telephone No. 8(495)531-64-81