Curriculum and Syllabi - 2016

M.TECH –VLSIDESIGN

Departmentof Electronics andCommunicationEngineering
Amrita School of Engineering

Very Large Scale Integrated (VLSI) Circuit Design is the process of designing a large computer chip (more specifically, an integrated circuit, or IC), using computer-aided design (CAD) tools on a workstation or a personal computer (PC). The course demands learning the principles of VLSI design, designing and fabricating the state of-the-art VLSI chips, understanding the complete design flow and expertise to design CMOS chips for industrial requirements. The curriculum focuses on employing hierarchical design methods and understanding the design issues at the various levels of hierarchy. Students are exposed to various design software in this programme. Also, they learn to design, simulate, implement and test complex digital systems using FPGAs (Field Programmable Gate Arrays). The main objectives of this course are to analyze the electrical and design characteristics of transistors, gates and to study the issues and methodologies involved in the integration of these devices into complex high-performance systems.

With recent and rapid upsurge in the areas like hardware software co-design, architectures for machine intelligence, network on chip etc. the programme is designed to cater to the needs in producing engineers trained in both hardware and software areas bridging the gap between the academia and industry. Students will be trained in several topics that cut across different domain, starting from lowermost level of physical devices to the top level of application development.

M. Tech. VLSI Design Programme
Curriculum – 2016

First Semester

Course code	Type	Subject	L	T	P	Credits
16MA616	FC	Mathematical Foundations for VLSI Design	3	0	1	4
16VL602	FC	Solid State Devices	3	0	0	3
16VL611	SC	CMOS Integrated Circuits	3	0	1	4
16VL612	SC	Digital System Design	3	0	0	3
16VL613	SC	Analog VLSI Design	3	0	1	4
16VL621	SC	VLSI Design Laboratory – I	0	0	2	2
16HU601	HU	Cultural Education*				P/F
Credits						20

* Non-credit course

Second Semester

Course code	Type	Subject	L	T	P	Credits
16VL614	SC	Functional Verification	3	0	0	3
16VL615	SC	VLSI Signal Processing	3	0	0	3
16VL616	SC	Design for Test and Testing	3	0	0	3
	E	Elective I	3	0	0	3
	E	Elective II	3	0	0	3
16VL622	SC	VLSI Design Laboratory –II	0	0	2	2
16VL797	P	Research Methodology	0	0	2	2
16EN600	HU	Technical Writing*				P/F
Credits						19

* Non-credit course

Third Semester

Course code	Type	Subject	L	T	P	Credits
	E	Elective III	3	0	0	3
	E	Elective IV	3	0	0	3
16VL623	SC	Open lab/Live-in Lab	0	0	1	1
16VL798	P	Dissertation				6
Credits						13

Fourth Semester

Course code	Type	Subject	L	T	P	Credits
16VL799	P	Dissertation				14

Total Credits: 66

Foundation Core

Course code	Type	Subject	L	T	P	Credits
16MA616	FC	Mathematical Foundations for VLSI Design	3	01		4
16VL602	FC	Solid State Devices	3	0	0	3

Subject Core

16VL611	SC	CMOS Integrated Circuits	3	0	1	4
16VL612	SC	Digital System Design	3	0	0	3
16VL613	SC	Analog VLSI Design	3	0	1	4
16VL621	SC	VLSI Design Laboratory – I	0	0	2	2
16VL614	SC	Functional Verification	3	0	0	3
16VL615	SC	VLSI Signal Processing	3	0	0	3
16VL616	SC	Design for Test and Testing	3	0	0	3
16VL622	SC	VLSI Design Laboratory –II	0	0	2	2
16VL623	SC	Open lab/Live-in Lab	0	0	1	1

Project

16VL797	P	Research Methodology	0	0	2	2
16VL798	P	Dissertation-Phase I				6
16VL799	P	Dissertation-Phase II				14

Elective Subjects

Course Code	Course	L T P	Cr
16VL701	Embedded System Design	3 0 0	3
16VL702	CMOS RFIC Design	3 0 0	3
16VL703	Nano Electronics	3 0 0	3
16VL704	VLSI Signal Conditioning	3 0 0	3
16VL705	VLSI Architectures for Multi-Core and Heterogeneous Computing	3 0 0	3
16VL706	Hardware Software Co-design	3 0 0	3
16VL707	VLSI Hardware Security and Trust	3 0 0	3
16VL708	Reconfigurable Computing	3 0 0	3
16VL709	Electronic System Level Design	3 0 0	3
16VL710	Low Power VLSI Circuits	3 0 0	3
16VL711	Network on Chip	3 0 0	3
16VL712	Wavelets and Applications	3 0 0	3
16VL713	Semiconductor Memory Design	3 0 0	3
16VL714	Static Timing Analysis	3 0 0	3
16VL715	Optoelectronic Devices	3 0 0	3
16VL716	VLSI Fabrication Technology	3 0 0	3

16VL717	Physical Design of Integrated Circuits	3 0 0	3
16VL718	Mixed Signal VLSI Design	3 0 0	3
16VL719	Communication Systems and Networks	3 0 0	3
16VL720	Optimization Methods	3 0 0	3
16VL721	Electronic Packaging and Reliability	3 0 0	3
16VL722	MEMS Design and Fabrication	3 0 0	3
16VL723	Emerging Architectures for Machine Learning	3 0 0	3

16MA616 MATHEMATICAL FOUNDATIONS FOR VLSI DESIGN 3-0-1-4

Objectives:

- To introduce basic concepts of linear algebra and Probability.
- To demonstrate the graduate students the application of linear algebra and probability in circuit theory and design.

Keywords: LTI, Matrix, Eigen Values, Probability, Markov, Poisson, Graph, Trees, Cycle.

Contents:

Matrices And Systems of Linear Equations –Vector Spaces over General Fields – Subspaces – Linear Independence – Basis – Dimension–Determinants–Linear Transformations – Associated Matrices – Change of Basis – Dimension Formula –Dual Vector Spaces –EigenValues – EigenSpaces – Diagonalization–Jordan Canonical Form –Inner Product Spaces – Bilinear – Quadratic and Hermitian Forms –Adjoint– Self-Adjoint– Orthogonal and Unitary Operators – DiagonalizationinEuclidean and Unitary Spaces –the Spectral Theorem –Probability–Basic Concepts– Random Variables – Mass and Density Functions – Conditional Probability –Bayes' Formula – Independence–Expectation– Moments– Generating Functions – Characteristic Function –Markov's Inequality –ChebyshevsInequality –Conditional Expectation – Independence –Correlation–Special Distributions and their Generating Functions – Binomial – Poisson – Normal – Linear Combinations of Normal Variables – Exponential – Raleigh– Functions of Random Variables and Transformations –Limit Theorems – Types of Convergence (Almost Sure, In Probability, In Distribution, L_p) – Continuity Theorem – Central Limit Theorem – Law of Large Numbers–Graphs–Isomorphism – Sub-Graphs –Degree – Matrix Representations – Cycles – Connectivity – Trees – Minimum Spanning Trees – BipariteGraphs – ChordalGraphs – EulerianGraphs – Hamilton Cycle – Dirac's Theorem – Planar Graphs – Euler's Formula – Basic Non-Planar Graphs – Graph Colorings – Greedy Colorings – Brooks Theorem.

TEXT BOOKS / REFERENCES:

1. Gilbert Strang, *Linear Algebra and its Applications*, FourthEdition, CengageLearning, 2006.
2. David C. Lay, Steven R. Lay and Judy J. Mc Donald,*Linear Algebra and itsApplications*, FifthEdition, Pearson, 2014.
3. Athanasios Papoulis, andS. UnnikrishnaPillai, *Probability, Random Variables, and Stochastic Processes*,Fourth Edition, Tata McGraw-Hill, 2002.
4. D. B. West, *Introduction to Graph Theory*, Second Edition, Prentice Hall, 2001.

Outcome:

- Students will be able to apply basic algebra and probability concepts in circuit analysis and design.

16VL602 SOLID STATE DEVICES 3-0-0-3

Objectives:

- Understanding the basic semiconductor device physics including quantum effects
- To understand operational principles of devices such as MOSFET etc.
- Use of MOSFET Models directly in to the circuit simulators for Analog/RF/Digital systems

Keywords: Quantum Mechanics, Built-in Potential, Sub-Threshold Characteristics, Silicon-on-Insulator, Small Signal Model.

Contents:

Review of Semiconductor Structure and Quantum Mechanics – Energy Bands and ChargeCarriers in Semiconductors – Doping and Carrier Concentration – Fermi Energy – Drift and Diffusion Currents– Transport Equation – Carrier Generation and Recombination – Excess Carriers –Diffusion of Carriers and Recombination – Continuity Equation – Ambi-polar Transport– Introduction to pn junction- built-in potential in Equilibrium – Forward and Reverse Bias – bias conditions–Heterostructures such asGaN– Metal-Semiconductor Junctions – The Ideal MOS Capacitor –Effect of Real Surfaces – MOSCAP Characteristics – MOSFET Characteristics – ThresholdVoltage – Mobility – Substrate Bias– Introduction to Large Signal model – MOSFET parasitic capacitances– small signal model – small-signal high frequency model, MOSFET Scaling and– Short-channel Effects– Sub-threshold Characteristics –DIBL - GIDL – MOSFET as MOS-Varactors– Silicon-on-Insulator MOSFET –Fundamentals of BJT – Amplification –Gummel-Poon/Mextram BJT models – Charge Control Analysis –Non-ideal Effects – Small Signal High Frequency Model.

TEXT BOOKS / REFERENCES:

1. D.A. Neamen, *Semiconductor Physics and Devices: Basic Principles*, Third Edition, McGraw-Hill International, 2003.
2. B.G. Streetman and S.K. Banerjee, *Solid State Electronic Devices*, Seventh Edition, PrenticeHall India, 2010.
3. Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Second Edition, CambridgeUniversity Press, 2009.
4. S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, Third Edition, John Wiley andSons Inc., 2007.

Outcomes:

- Ability to use the MOSFET for DC IV, CV characteristics.
- Ability to do simulations of Analog/RF/Digital circuits and systems.

16VL611 CMOS INTEGRATED CIRCUITS 3-0-1-4

Objectives:

- To introduce the basic concepts of MOS transistors.
- To provide a platform for transistor level digital circuits design.
- To learn and practice different logical implementation and their significances.

Keywords: PMOS, NMOS, Static, Transmission Gates, Switching Threshold, Rise/Fall Time, Delay, Sizing, Pseudo, Dynamic, Logical Effort.

Contents:

NMOS and PMOS Transistors – Threshold Voltage – Body Effect – Second-order Effects – NMOS and CMOS Inverters – Inverter Ratio – DC and Transient Characteristics – Switching Times – Driving Large Capacitance Loads – CMOS Logic Structures – Transmission Gates – Static CMOS Design – Dynamic CMOS Design – Parasitic Estimation – Switching Characteristics – Transistor Sizing – Power Dissipation and Design Margining – Charge Sharing – Logical Effort – Scaling – Combinational Circuits. Interconnects – Electro static discharge (ESD) – Latch-up and its Prevention – Introduction to Sequential Circuit Design and Timing Analysis–**Lab**: Measuring Transistor Parameters Using Simulation Tools– VTC for Inverters– NAND and NOR – Measuring Switching Threshold–Rise Time– Fall Time – Delay Time – Power and Noise Margin for an Unit Inverter – Inverter Chain– Comparison Between Different Logic Styles.

TEXT BOOKS / REFERENCES:

1. Jan M. Rabaey, Anantha P. Chandrakasan and BorivojeNikolić, *Digital Integrated Circuits: A Design Perspective*, Second Edition, Prentice Hall India, 2003.
2. Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits - Analysis and Design*, Third Edition, Tata McGraw-Hill, 2003.
3. Neil H. E. Weste and David Money Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison Wesley, 2010.

Outcomes:

- Ability to design basic digital circuits in transistor level.
- Ability to choose the suitable logical styles for the given problems.
- Ability to analyse the transistor level circuits.
- Ability to measure delay and find optimized delay.

16VL612 DIGITAL SYSTEM DESIGN 3-0-0-3

Objectives:

- To design and synthesize integrated circuits using programmable hardware such as FPGAs
- To convert an electronic design concept to register transfer level (RTL).
- To develop HDL models of combinational and sequential circuits and verification.

Keywords: Shift Registers, Memory, Multiplier, Finite State Machine, Arithmetic Processor, Synthesis and Simulation.

Contents:

Register Files – FIFOs – LIFOs – SIPOs – Bidirectional Shift Register – Universal Shift Register – Barrel Shifter – Linear Feedback Shift Registers – Memory – RAM – Static RAM – Dynamic RAM – Serial Access Memory – ROM – Content Addressable Memory – Booth Multiplier – Wallace Tree Multiplier – Baugh-Wooley Multiplier – Design and Synthesis of Data Path Controller – State Diagram to Control External Hardware Subsystems and Synthesis – Synchronous and Asynchronous FSM Design – Programmable Logic and Storage – Algorithm and Architecture for Digital Arithmetic Processor Design –Post Synthesis Design-Principles of Asynchronous Interaction – Handshake Protocols –Muller C Element – Simple Pipelines – Speed-Independence–Delay-insensitivity – Classes of Asynchronous Circuits –Delay models – Asynchronous Design Methodologies and Building Blocks–Completion Indicators – Synchronizers –Arbiters– Delay Insensitive Codes–Globally Asynchronous Locally Synchronous (GALS) Designs–Synthesis of Asynchronous Control Logic– Design Techniques for Low Power in Deep-submicron Systems and Technologies.

TEXT BOOKS / REFERENCES:

1. Michael D. Ciletti,*Advanced Digital Design with Verilog HDL*, Second Edition, Pearson Higher Education, 2011.
2. Morris Mano and Michael D. Ciletti,*Digital Design: With an Introduction to the Verilog HDL*, Fifth Edition,Pearson Higher Education, 2013.
3. Peter Minns and Lan Elliott,*FSM Based Digital Design Using Verilog* HDL, Fifth Edition, John Wiley and Sons Ltd, 2008.
4. Parag K. Lala, *Principles of Modern Digital Design,*Second Edition, John Wiley and Sons Ltd., 2007.

Outcomes:

- Understand advanced topics in digital logic design.
- Understand modeling and verification with hardware description languages.
- Design state machines and datapath controllers.

16VL613 ANALOG VLSI DESIGN 3-0-1-4

Objectives:

- To provide exposure in using device models, biasing circuits, small-signal operations, high frequency performance analysis and op amp design concepts.
- To use circuit simulators in the design of electronic circuits based on active devices (particularly MOS device)anddetermination of circuit parameters.

Key words: MOS Theory, Small Signal and Large Signal Models, SPICE Models, MOS Amplifier Topologies, High Frequency Response, Frequency Compensation, Oscillators.

Contents:

MOS Large-signal and Small-signal–High-frequencyModeling– Short-Channel–Sub-threshold Operation –Leakage Current – MOS Diodes – Active Resistors – Capacitors– Current Sink and Source–Cascade and CurrentMirrorsConfigurations–Gain-boosting– Current and Voltage references–MOS Inverters – Active Load – Current Source – Push-Pull – Frequency Response– Single-stage MOS Amplifiers –Miller Effect–High-frequencyEffects–MOSSmall-signalModel of Amplifiers–DifferentialAmplifiers–Active Loaded DifferentialPair–FeedbackAmplifiers– Negative Feedback – Dynamic Response – Inverting and Non-Inverting Amplifiers–LoopGain– Two-Stage CMOSOp-amp – Performance Study of GainandFrequencyResponse – Compensation– Comparators–Oscillators – Quadrature VCO–**Lab:**DC– I-V– C-V and $g_m$of MOSFET –S-parameter Simulation Using SPICE/BSIM-4 models –Current Mirrors–Amplifier Topologies with Active Load–Differential AmplifierConfigurations.

TEXT BOOKS / REFERENCES:

1. B.Razavi,*DesignofAnalogCMOSIntegratedCircuits*,TataMcGraw-Hill,2002,(Reprint 2015).
2. P.E.AllenandD.R.Holberg,*CMOSAnalogCircuitDesign*,ThirdEdition,OxfordPress, 2011.
3. P.R.Gray,P.J.Hurst,S.H.LevisandR.G.Meyer,*AnalysisandDesignofAnalogIntegratedCircuits*,JohnWileyandSons Inc., 2009.
4. T.C.Carusone,D.A.Johnsand, K.W.Martin,*AnalogIntegrated Circuit Design*,Second Edition, John WileyInc,2012.

Outcomes:

- To make expertise in SPICE based circuit simulators
- Ability to design active loaded (IC), MOS based single/multi-stage, operational amplifier considering terminal impedance matching.

16VL621 VLSI DESIGN LABORATORY-1 0-0-2-2

Objectives:

- To Build basic designs and incorporate them into system level design.
- To do experiments using FPGA and other tools for various digital designs.

Keywords: Timing Diagrams, Synthesis Aspects, FPGA and ASIC Libraries, VLSI Tools, Simulation,Synthesis.

Contents:

Basic digital designs for combinational and sequential logic implanted in all coding styles in HDL and check for functionality and determine the timing, area report.
State machine Design.
System level design case studies.
Demonstration of RTL design and their role in synchronization and timing to understand slack, timing.

TEXT BOOK/REFERENCE:

1. Lab Manuals and online manuals for tools usage and LanguagereferenceManuals of HDLs.

Outcomes:

- Ability to implement the designs using front end design environment using top down and bottom up approach.
- Ability to verify the functionalities of the designs
- Ability to analyse the area, delay trade-offs and performance metrics associated with simulation and synthesis.

16VL614 FUNCTIONAL VERIFICATION 3-0-0-3

Objectives:

- To introduce verification of hardware designs.
- To provide a hands-on feel for verification of designs.
- Togive an introduction to FPGA based verification and Emulation of VLSI systems

Keywords: Verification, Randomization, Direct Programming Interface, Assertions Based Verification, OVM & UVM.

Contents:

Introduction to Verification– Need for Functional Verification –Validation andEmulation – ASIC Verification Concepts– Bottle Neck Problem in ASIC DesignChallenges – Design – FPGA and Emulation based Validation and Testing – MajorVerification Tasks – Creating Verification Plan – LinearTest Bench – Linear Random Test Bench– Self Checking Test Benches – Test CoverageFormal Verification–Decision Diagrams – Equivalence Checking – Symbolic Simulation –Model Checking – Symbolic ComputationSystemVerilog for Design– Standard Data Types and Literals –Procedures and Procedural Statements –Operators– User-Defined Data Types – Hierarchy and Connectivity –Tasks and Functions –Interfaces – SystemVerilog for Verification–Verification Blocks –Transaction– Level Modeling– SystemVerilog Classes – Random Stimulus – Class-Based Randomization – Functional – Coverage – Queues and Dynamic Arrays– Interprocess Synchronization – Direct Programming Interface (DPI) SystemVerilog Assertions– Assertion-Based Verification (ABV) – Immediate and Concurrent Assertions – Simple Boolean Assertions – Sequences –Sequence Composition – Advanced SVA Features – Coding Guidelines– Functional Coverage -Practical SVA Application – Introduction to Static Formal Verification–OVM/UVM Verification Componentsand Objects – OVM/UVM Transactions –OVM/UVM Factory Basics

TEXT BOOKS / REFERENCES:

1. Chris Spear, *SystemVerilog for Verification: A Guide to Learning the TestBenchLanguage Features*, Third Edition, Springer, 2012.
2. Douglas Perry, andHarry Foster, *Formal Verification: For Digital Circuit Design*, First Edition, McGraw-Hill Education, 2005.
3. S Halsoun and T Sasao, *Logic Synthesis and verification*, Kluwer Academic publishers, 2002.
4. PallabDasgupta, *ARoadMap for Formal Property Verification*, Springer 2006.

Outcomes:

- Ability to familiarize verification process and its different methodologies.
- Ability to write test-benches using system verilog in an efficient way.
- Ability to develop algorithms which can automate the design verification process.

16VL615 VLSI SIGNAL PROCESSING 3-0-0-3

Objectives:

- To introduce concepts in the design and implementation of DSP architectures.
- To realize architectures with high throughput, less area and less power.

Keywords: FIR Filter, IIR Filter, Pipelining, Parallel Processing, Folding, Retiming, Systolic.

Contents:

Introduction to Digital Signal Processing Systems – Iteration Bound – Pipelining and Parallel Processing – Retiming – Unfolding – Folding – Systolic Architecture Design – Pipelined and Parallel Recursive and Adaptive Filters–Scaling and Round off Noise –Digital Lattice Filter Structures – Bit-Level Arithmetic Architectures – Programmable Digital Signal Processors – Computational Accuracy in DSP Implementations – Adaptive Filters–Kalman Filters.

TEXT BOOKS/REFERENCES:

1. Keshab K. Parhi, *VLSI Digital Signal Processing Systems, Design and Implementation*, Wiley, 1999.
2. Venkataramani B and Baskar M., *Digital Signal Processors, Architecture, Programming and Applications*, Tata McGraw-Hill, 2002.
3. Avatar Singh and Srinivasan S., *Digital Signal Processing Implementations Using DSP Microprocessors with Examples from TMS320C54X*, Thomson Learning, 2004.
4. Simon Haykin, *Adaptive Filter Theory*, Prentice Hall, 1997.

Outcomes:

- Ability to implement basic digital signal processing blocks like FIR and IIR filters.
- Ability to optimize the design by employing various algorithms.

16VL616 DESIGN FOR TEST AND TESTING 3-0-0-3

Objectives:

- To introduce the concept of VLSI Testing and analyze the potential of ATPG algorithms.
- To design for testability and explore the built-in-test concepts.
- To learn and understand the challenges involved in scan design and test.

Key words: VLSI Testing, Design for Testability, Automatic Test Pattern Generation, Built-in-self-test, Boundary Scan

Contents:

Testing of VLSI Circuits– Fault Modeling – Equivalence and Dominance - Logic and Fault Simulation –Testability Measures – ATPG Fundamentals – Combinational Circuit Test Generation – Redundancy Identification – ATPG for Roth's D-algorithm – PODEM – Sequential Circuit Test Generation – Time Frame Expansion and Implementation – Design for Testability– Scan Architectures and Testing –Pseudo Random Testing – Testable Combinational Logic Circuit Design – Design of Testable Sequential Circuits–BIST Architectures –Test-Per-Clock – Test-Per-Scan BIST Systems – Memory BIST – DFT Fundamentals –At-speed Testing – Boundary Scan Architecture – JTAG Standards.

TEXT BOOKS / REFERENCES:

1. Vishwani D. Agrawal and Michael L. Bushnell, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Kluwer Academic Publishers, 2000.
2. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan &Claypool Publishers, 2009.
3. LaungTerng Wang, Cheng Wen Wu and Xiaoqing Wen, *VLSI Test Principles and Architectures – Design for Testability*, First Edition, Morgan Kaufmann Publishers, 2006.
4. MironAbramovici, Melvin A. Breuer andArthur D.Friedman, *Digital Systems Testing and Testable Design*, Jaico Publishing House, 2001.

Outcomes:

- Improves the knowledge level in the domain of VLSI Design and Test
- Enhances the creativity to develop new ATPG Algorithms
- Enables the student to design for testability

16VL622 VLSI DESIGN LABORATORY-1I 0-0-2-2

Objective:

- To use advanced tools to study front end and back end implementations.
- To build custom circuits using analog and digital environments.

Keywords: Area, Delay, Layout, Power, Timing Analysis, Digital, Analog Circuits Simulation and Analysis

Contents:

Data Path Circuits–State Machine in Front End for Simulation –Synthesis –Area and Delay Tradeoff–LayoutRepresentation and Circuit Extraction in Backend.
Analog Circuits and Mixed Signal Circuit Simulation and Analysis.
Timing and Power Analysis of Standard Combinational and Sequential Circuits.

TEXT BOOKS/REFERENCES:

1. Lab Manuals and online manuals for tools usage and Language reference Manuals of HDLs.

Outcomes:

- Ability to analyze the circuits built in simulation, synthesis, timing and layout environments using VLSI tools from standard EDA companies.
- Ability to interface between front end and backend design flows.
- Post layout extraction and simulation.

16VL797 RESEARCH METHODOLOGY 0-0-2-2

Objectives:

- To learn and practice the literature survey aspects of projects and prepare the scope and goals for the proposed project.
- To learn, practice and improve the research presentation skills and with latest tools
- To learn and understand the research publication ethics and tools like LaTeX.

Key words: Plagiarism, Seminar, LaTeX, Journal, Ethics, Scopus, Science Citation, Web of Science, Thomson Reuters, H-index

Contents:

Logical Thinking – Approach Towards Analytical Probing – Defining Problems – Perceptive Views of Conclusions –Selection of Project Domain – Allocation of Project Supervisor/ Mentor –Publication Ethics–Tools and Evaluation –Basic Components of a Research Paper – Procedures and Processes –Journal Types–Scopus– Web of Science –Thomson Reuters–Science Citation Index–H-Index –Google Citations–Selection of Tentative Project Area Process of Literature Survey – Literature Survey Components and Procedures–Presentation of Selected Project Proposal – Oral Presentation Preparation of a Report on the Selected Project Proposal in LaTeX

Format–Evaluation Components (Campus Specific) –Attending Special Invited Lectures – Practical Orientation in Searching and Collecting Literature – Online Tools– Presenting a Seminar on Selected Project Proposal –and Submitting Project Report Prepared Using LaTeX.

TEXT BOOK / REFERENCE:

1. ManavAggarwal, *Research Methodology Trends & Techniques*, Neha Publishers & Distributors, 2012, ISBN10: 9380902111
2. www.csus.edu/indiv/d/**dowden**b/4/**logical-reasoning**.pdf

Outcomes:

- Enable the student potentials to organize, coordinate and focus the research aptitude with confidence.
- Improve the awareness on indexing, quality evaluation, author index of publications
- Improve the presentation skills through seminars
- Expertise in LaTeX tool for report preparation

16EN 600 TECHNICAL WRITING P/F

(Non-credit Course)

Technical terms – Definitions – extended definitions – grammar checks – error detection – punctuation – spelling and number rules – tone and style – pre-writing techniques – Online and offline library resources – citing references – plagiarism – Graphical representation – documentation styles – instruction manuals – information brochures – research papers – proposals – reports (dissertation, project reports etc.)

TEXTBOOKS/REFERENCES:

1. H.L. Hirsch, *Essential Communication Strategies for Scientists, Engineers and Technology Professionals*, Second Edition, New York: IEEE press, 2002.
2. P.V. Anderson, *Technical Communication: A Reader-Centered Approach*, Sixth Edition, Cengage Learning India Pvt. Ltd., New Delhi, 2008, (Reprint 2010).
3. W.Jr. Strunk and E.B.White, *The Elements of Style*, New York. Alliyan & Bacon, 1999.

16VL623 OPEN LAB / LIVE-IN LAB 0-0-1-1

Objectives:

- To design, develop and realize new experiments for the program, including practical manuals.
- To introduce the students to provide technical solutions for real world problems and develop proto-type systems through Live-In labs.

Keywords: Technical solutions, real world problems, proto-type systems, Live-In labs.

Contents:

Selection of lab /tool / domain
Evaluation of proposed concept and its requirements / Timeline
Final evaluation of the proposal and demonstration of the proposed system
Evaluation of the manual / report / accuracy and importance
Review on Patentability / Publication potentials on the system
Evaluation components (Campus specific): Review team to evaluate (one time) the authenticity of the project / Lab experiment options/ utilization of existing lab tools / manual preparation / demonstration of hardware/software.

Outcomes:

- Enable the students' potentials to realize a proto-type system
- New experiments utilizing the full potential of the lab facilities for future students
- Improve the confidence and understanding of the concepts in practical aspects

16VL798 DISSERTATION 0-0-0-6

Objectives:

- To select the problem definition of the proposed work
- To define the objectives of the proposed work
- To define the components of the work
- To define the timeline and deliverables of the phase I

Key words: Literature survey, Scientific research, Problem definition, objectives of the proposal, Timeline/schedule, Deliverables, Implementation, experimental results, performance analysis, result, inference, conclusion.

Contents:

Selection of project domain
Literature survey
Problem statement, Objectives, Deliverables
Presentations
Implementation, results analysis and inference
Publishing and Report writing

Evaluation components (Campus specific): Selection of project or problem definition, presentation in regular reviews for acceptance of the proposal, feasibility and implementability of the proposal, fine tuning of the objectives and deliverables. Evaluation of the attained deliverables of the work, publication and report submitted at the end of phase I of the Dissertation

Outcomes:

- Enable to develop the problem definition through extensive literature survey.

- Enable to implement the work by appropriate selection of methodology and tools.
- Enable to prepare a publication for Conference/Journal.

16VL799 DISSERTATION 0-0-0-14

Objectives:

- To continue with problem definition of phase I or extend the problem definition of the proposed work in phase I
- To augment the objectives of the proposed work
- To augment the scope and the components of the work
- To come out with intensive work components, their timelines and deliverables

Key words: Literature Survey, Scientific Research, Problem Definition, Objectives of the Proposal, Timeline/Schedule, Deliverables, Implementation, Experimental Results, Performance Analysis, Result, Inference, Conclusion.

Contents:

Augment the scope of problem definition
Literature survey
Problem statement, Objectives,
(Augmented if any additional from phase I)
Presentations
Implementation, results analysis and inference
Publishing and Report writing

Evaluation components (Campus specific): Selection of project or problem definition, extension of scope possibility based on the requirement. Presentation in regular reviews to evaluate and fine tune the progress of the work and the deliverables. Evaluation of the attained deliverables of the work, publication and report submitted at the end of phase II of the Dissertation with a final external review.

Outcomes:

- Enable to develop the problem definition through extensive literature survey and discussions with guide/supervisor
- Ability to organize, and plan the work components of the proposed work
- Ability to implement the work by appropriate selection of methodology and tools
- Ability to analyse the Outcomes of their project by formulation critical performance measures for comparison with state of art
- Enable to develop a manuscript for publication and report.

16VL701 EMBEDDED SYSTEM DESIGN 3-0-0-3

Objectives:

- To learn the architecture of ARM Cortex-M Microcontroller for embedded design.

- To practice embedded software programming using KEIL platform.
- To learn and understand various design and implementation of simple embedded systems.

Keywords: Microcontroller, ARM, Embedded Systems, Software Architecture, RTOS, Semaphores, PLL, UART, Timer, ADC, DAC, Interrupts, Device Drivers.

Contents:

Microcontroller Fundamentals – ARM–ASM Programming and basics of C – I/O Interfacing (LED and Switch) – Microcontroller Ports – Design and Development Process Architecture – Micro-architecture – Design – Implementation – Verification and Validation – Development Tools – Block Diagrams – Flowcharts – Call Graphs – Dataflow Graphs – Finite State Machines – Parallel Interface – GPIO – Serial Interface – UART – PLL Programming – Timer – Fixed Point Software – Structs – Stacks and Recursion using ASM Programming – Device Driver – Interfacing with a Hitachi HD XXX Display – I/O Synchronization – Interrupts – DAC – Music Synthesis and Music Playback – ADC – Real-world Interfacing and Data Acquisition – Applications using ADC– DAC – Interrupts – UART–Display Device Driver – Memory Management in Embedded Systems – Shared Data Problem – RTOS.

TEXT BOOKS/REFERENCES:

1. Jonathan Valvano,*Embedded Systems: Introduction to ARM® Cortex™-M Microcontroller*, Volume 1, Fourth Edition, Create Space Independent Publishing Platform, 2012.
2. Arnold S. Berger, *Embedded System Design*, First Edition, CRC Press, 2001, (Reprint 2002).
3. David E. Simon, *An Embedded Software Primer*, First Edition, Pearson Education,2001.
4. Steve Heath,*Embedded Systems Design*, Second Edition, Newnes, 2002.

Outcomes:

- Ability to understand any other microcontrollers.
- Ability todesign an optimised system considering both software and hardware aspects.
- Ability to analyse the necessity of a particular hardware.

16VL702 CMOS RFIC DESIGN 3-0-0-3

Objectives:

- To learn the design of CMOS RF IC needed to build Transceiver (Transmitter and Receiver) for mobile/satellite/defense communication.
- To get hands-on training of designing of RF/Analog IC Design in Lab.

Keywords: Small Signal Model, Noise Analysis, Low Noise Amplifier, Broadband Amplifier, RF Oscillators, Mixers, Power Amplifiers.

Contents:

Small Signal RF Model of MOSFET – Noise in MOSFET and in Circuit – Non-linearity – 1-dB Gain Compression Point – InterModulation and IIP3/OIP3 – Dynamic Range – Sensitivity –RF

Transmitter and Receiver Architectures with Hartley Architecture of Receiver – Impedance Matching – RF Low Noise Amplifier – Design of Common Source – Common Gate –Cascode and Differential Configurations with Implementations by Inductors –Microstrip and CPW Transmission Lines – Broadband Monolithic Distributed Amplifier with CPW Inductive Transmission Lines – RF Oscillators –Ring Oscillator – LC Cross-Coupled/negative-resistance Oscillator – Distributed Oscillator and Voltage Controlled Oscillator (VCO) – Use of MOSFET as MOS-Varactors in VCO, Quadrature VCO – Phase Noise in Oscillators – RF Mixers – Active Down-conversion Mixers such as Single-Balanced – Double-Balanced/Gilbert Cell Mixers – Phase lock Loop (PLL) – Phase Frequency Detector (PFD) and Charge Pump (CP) – CP-PLL – PLL Integer-N Frequency Synthesizer – PLL Divider Chain with Injection-Locked Frequency Divider –Class E (stacked FET and others) Power Amplifiers for 60/77 GHz bands – Doherty Power Amplifier – Project Based Implementation Practices.

TEXT BOOKS / REFERENCES:

1. B Razavi, *RF Microelectronics*, Second Edition, Pearson, 2012 (Indian Edition 2013 by Dorling Kindersley).
2. SorinVoinigescu, *High-Frequency Integrated Circuits*, Cambridge University Press, 2013, South Asian Paperback edition of 2016.
3. Michael Steer, *Microwave and RF Design - A Systems Approach*, SciTech Publishing, 2010, Indian Reprint by Yesdee Publishing, 2012.
4. Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Second Edition, Cambridge University Press, 2004, Indian Reprint of 2009.

Outcomes:

- Ability to design Receiver using LNAs, Oscillators and Mixers.
- Ability to designtransmitterusing Power Amplifiers.
- Course Project on 60 GHz 5G Receiver/Doherty PA design and development in Lab.

16VL703 NANO ELECTRONICS 3-0-0-3

Objectives:

- To understand the latest trends in the technology and principles of nano-electronics.
- To familiarize new material devices and their performances.

Keywords: Quantum Well, Wire, Graphene, FINFETS, CNT.

Contents:

The Schrödinger Equation –Electrons in a Crystal Lattice – Quantum Well– Wire and Dot Devices — Phonons and Photons – Scattering Rates and Lifetimes in Electronic Devices –CVD and Other Processes in Fabrication of Nano Devices – Deep Submicron Devices Limits to Scaling –Nano Devices – Quantum Effects– Atomic Scale Parameter Fluctuation –the NanoscaleMOSFET –FINFETS –Vertical MOSFETS–Resonant Tunneling Transistors –Single Electron Transistors –and Spintronics Devices –Atoms–up Approaches – Transport in Molecular Structures – Molecular Systems as Alternatives to Conventional Electronics – Drift Diffusion– Ballistic Transport –NEGF – Molecular Interconnects – Graphene–Carbon Nanotubes and Silicon Nanowire Technology – Devices and Circuits –Spintronics– Band-

Structure and Transport – Devices – Applications –Innovative Device Architectures (Double–Gate MOS Transistor –Dynamic Threshold MOS Transistor –Gate–all–Around Transistor – Vertical MOS Transistors) –Nano-Scale and Quantum Devices –Single Electron Transistor (SET) – Quantum Wires – Few-Electron Memories–Steep Slope Switches –Tunnel FETS– Quantum Dot Cellular Automata (QCA).

TEXT BOOKS / REFERENCES:

1. C.P. Poole Jr., and F.J. Owens,*Introduction to Nanotechnology*, Wiley 2003.
2. WaserRanier, *NanoElectronics and Information Technology (Advanced Electronic Materials and Novel Devices)*, Wiley VCH, 2003.
3. K.E. Drexler, *NanoSystems*, Wiley, 1992
4. John H. Davies,*The Physics of Low-Dimensional Semiconductors*, Cambridge University Press, 1998.

Outcomes:

- Ability to understand the principles of scaling and limitations of silicon based devices and development of nano-electronic devices.
- Ability to use of wave – particle analysis in the development of transport properties.

16VL704 VLSI SIGNAL CONDITIONING 3-0-0-3

Objectives:

- To make the signal compatible for the next stage by manipulating the signal.
- To introduce Operational Trans-conductance amplifier and OTA based circuits.
- To understand g_m/I_D based designs and different signal conditioning circuits.

Keywords: OTA, g_m/I_D, Gm-C, NAUTA, Q – tuning, Biquads, Filtering, Amplification.

Contents:

Operational Trans-conductance Amplifier basic Considerations – Application Requirements for OTAs used in Filters – The Case for Fully Differential Circuits – Transistor Models – Gm/IDbased Design – Single-stage OTAs – Basic Differential Pair – Telescopic Architecture – Folded Cascode Architecture – Two-stage OTA – Gain Boosting – Common-mode Feedback Implementation– Gm-C Biquad – Trans-conductor Implementation – NAUTA Cell – Source Follower based Filter – Parameter Tuning – Q-tuning – VCF-tuning – Discrete Frequency Tuning / Programming – Tuning Gm over a Wide Range – Switched Capacitor Filters – Parasitic Sensitive Configurations – Transient and Circuit Analysis – Frequency Response – Aliasing – Periodic AC Analysis – SC Integrators – Martin-SedraBiquad – Low and High Design Q Biquads – Noise Analysis –Precision Analog Circuit Techniques –Applications.

TEXT BOOKS/REFERENCES:

1. Schauman, Rolf and Van Valkenburg, *Design of Analog Filters*, Second Edition, Oxford University Press, 2009.

2. Tony Chan Carusone, David A. Johns and Kenneth W. Martin, *Analog Integrated Circuit Design*, Second Edition, John Wiley Inc., 2012.
3. Gregorian and Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986.

Outcomes:

- Knowledge about gm/Id based design.
- Ability to Understand parameter tuning, filtering and various signal conditioning blocks.
- Ablility to design different signal conditioning circuits.

16VL705 VLSI ARCHITECTURES FOR MULTICORE AND HETEROGENEOUSCOMPUTING 3-0-0-3

Objectives:

- To understand the performance of multi-core processors and high-performancecomputing systems.
- To understand the architectural considerations and VLSI implementation details.
- To introduce advance computer architectural techniques.

Key words: Parallelism, Scheduling, Power, Energy

Contents:

Review of Types of Parallelism –Instruction Level Parallelism –Thread Level Parallelism – Limits of ILP–Parallel Processing Architectures –Superscalar–VLIW–Scheduling Techniques– Static and Dynamic Schemes –Inter-Processor Communication Schemes –Bus-Based– Shared Memory– Distributed Memory and Network on Chips –Performance Analysis–Understanding the Impact of the Architectural Modifications on Execution Time on Diverse Applications – Introduction to Markovian/Stochastic Models for Heterogeneous Computing–Operating System - Role of Multi-Cores –Case Study for Heterogeneous Architectures.

TEXT BOOKS / REFERENCES:

1. Hennesey and Patterson, *Computer Architecture*: *A Quantitative Approach*,Fifth Edition,Morgan Kaufmann, 2012.
2. K. Uchiyama, F. Arakawa, H. Kasahara, T. Nojiri, H. Noda, Y. Tawara, A. Idehara, K. Iwata and H. Shikano, *Heterogeneous Multi-core Processor Technologies for Embedded Systems*, Springer, 2012.
3. J. Dongarra and A.L. Lastovetsky, *High Performance Heterogeneous Computing*, Wiley Series, 2009

Outcome:

- Ability to analyze performance using state-of-the art simulator for multi-core architectures

16VL706 HARDWARE SOFTWARE CO-DESIGN 3-0-0-3

Objectives:

- To introduce the design of mixed hardware-software systems.
- To partition simple software programs into hardware and software components.
- To identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components

Keywords: Co-Design Models, SystemC, Scheduling, Co-Simulation.

Contents:

Introduction To System Level Design –Generic Co-Design Methodology–Hardware-Software Co-Design Models and Architectures –Language for System Level Specification Design and Modeling (SpecC, ArchC And SystemC) – Design Representation for System Level Synthesis – Models of Computation–Architectural Selection–Partitioning–Scheduling and CommunicationHardware– Software Co-Simulation–Synthesis–Verification and Virtual Prototyping Implementation Case Studies – Performance Analysis and Optimization – Re-Targetable Code Generation – FPGAS.

TEXT BOOKS / REFERENCES:

1. Patrick R. Schaumont,*A Practical Introduction to Hardware/Software Co-design*, Second Edition, Springer, 2013.
2. Jorgen Staunstrup and Wayne Wolf,*Hardware/Software Co-design: Principle and Practice*, Kluwer Academic Publishers, 1997.
3. Giovanni De Micheli, *Readings in Hardware Software Co-design*, Morgan Kaufmann, Academic Press, 2002.
4. Sao-Jie Chen, Kuang-Huei Lin, Pao-Ann Hsiung and Yu-Hen Hu, *Hardware Software Co-Design of a Multimedia SOC Platform*, Springer, 2010.

Outcomes:

- Ability to analyze hardware-software co-design problems for systems with moderate complexity.
- Apply hardware-software co-design methods and techniques to practical problems.
- Applying different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.

16VL707 VLSI HARDWARE SECURITY AND TRUST 3-0-0-3

Objectives:

- To explore the various security threats in ICs.
- To know various countermeasures to address security threats.

Keywords: Trojan Attacks, Detection and Isolation, Side-channel Attacks, Physically Unclonable Functions, Trusted Platform Modules.

Contents:

Integrated Circuits (IC) Trojans – Vulnerabilities in Combinational and Sequential Logic – Finite State Machines – Trojan Attacks – Detection and Isolation – Side-channel Attacks include Power Spectrum Analysis – EM Analysis – Timing Analysis – Fault Injection- FPGA Security Attacks such as Hardware Trojans in Bit Files – Physical Attacks on FPGA – Physical Design Layers – Emerging Hardware Security and Trust – Trusted Platform Modules (TPM) for Hardware – Physically Unclonable Functions (PUFs) – True Random Number Generators (TRNG) – RFID Tag-Hardware System Tampering – Tamper Resistant Hardware Design Techniques – Anti-Counterfeiting for Microelectronics Devices – Protection of Intellectual Property (IP) – Discussions on IC Reverse Engineering – Methods to Make Reverse Engineering Harder – Non-standard Cell Libraries – Reduction in Feature Sizes.

TEXT BOOKS/REFERENCES:

1. M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust*, Springer, 2011.
2. J. Plusquellic, *Trojan Taxonomy*, University of New Mexico,http://www.ece.unm.edu/~jimp/HOST.
3. D. Agrawal, S. Baktir, D. Karakoyunlu, P. Rohatgi and B. Sunar, *Trojan Detection using IC Fingerprinting*, IEEE, Symposium on Security and Privacy, 2007.
4. G. Edward Suh and S. Devadas,*PhysicalUnclonable Functions for Device Authentication and Secret Key Generation*, DAC-2007.

Outcomes:

- Ability to understand effects of hardware trojans.
- Ability to understand the difficulties in detecting and identifying security threats.
- Ability to understand various techniques for trusted designs.

16VL708 RECONFIGURABLE COMPUTING 3-0-0-3

Objectives:

- To introduce architecture that enables high performance computation as well as the supporting application mapping process.
- To familiarize wide range of reconfigurable architectures.
- To explore different opportunities for the use of reconfigurable architectures.

Key words: FPGA, Reconfiguration, high-level synthesis

Contents:

Reconfigurable Computing Hardware –Survey of FPGA and non-FPGA devices – Fine-grained – Coarse-grained - Reconfiguration Management – Partial and Dynamic ReconfigurationProgramming– Reconfigurable Computing Systems–Mapping Applications to Reconfigurable Systems –High-level Synthesis–Area-Performance – Power-aware Mapping–Placement – Layout and Routing–Application Development–Case study with Applications and Solutions from Different Domains.

.

TEXTBOOKS / REFERENCES:

1. Scott Hauck and Andre Dehon, *Reconfigurable Computing: The Theory and Practice of FPGA Based Computation*, Elsevier, 2008.
2. Christophe Bobda, *Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications*, Springer 2007.

Outcomes:

- Ability to understand the fundamentals of FPGA and non-FPGA reconfigurable architectures and design.
- Explore to the state-of-the-art tools in reconfigurable computing

16VL709 ELECTRONIC SYSTEM LEVEL DESIGN 3-0-0-3

Objectives:

- To learn virtual prototyping.
- To familiarize SystemC based design and debug
- To learn the basics of Transaction Level Modelling and High Level Syntheis
- To familiarize on Accrellera consortium, its activities and standards

Keywords: Electronic System level design, Architecture Exploration, Open Source Languages,SystemC, ArchC, SpecC, Virtual Platform, Virtual Prototyping, Transaction Level Modelling, High level Synthesis and Accellera.

Contents:

Introduction to Electronic System Level Design– Hybrid Design – ESLD Flows and Methodologies – Architecture Exploration–Hardware-software Partitioning– Models for ESLDesign– Open Source Languages–SpecC–ArchC and SystemC for ESLD– Transaction Level Modelling Building Platform Models in SystemC– High Level Synthesis– ESL Verification – Virtual Platform and Virtual Prototyping– Debugging SystemC Platform Models – SystemCBasedPower Evaluation –SystemCStandards and AccelleraInitiatives ESLD – Project Based Practice design.

TEXT BOOKS / REFERENCES:

1. SandroRigo, Rodolfo Azevedo and Luizsantos, *Electronic System Level Design – An Open Source Approach*, Springer, 2011.
2. Brian Bailey and Grant Martin, *ESL Models and their Application in Electronic System Level Design and Verification in Practice*, Springer, 2010.
3. Daniel Grobe and Rolf Drechsler, *Quality Driven SystemC Design*, Springer, 2010.
4. Mark Burton and Adam Morawiec, *Platform Based Design at Electronic System Level – Industry Perspectives and Experience*s, Springer, 2006.

Outcomes:

- Basic knowledge of ESD.
- Ability to design systems using SystemC.

16VL710 LOW POWER VLSI CIRCUITS 3-0-0-3

Objectives:

- To provide a comprehensive idea about different sources of power dissipation in VLSI circuits.
- To introduce power estimation methods.
- To understand different power optimization methods and challenges.

Keywords: Static power, switching power, short circuit power, probability, low power designs.

Contents:

Importance of Low Power Consumption – Design for Low Power – Deep Submicron and Nanometer MOS Transistors and Models – Sources of Static and Dynamic Power Consumption in MOS Devices – New Device Technologies for Reducing Leakage Current – Basics of Power and Energy – Power Optimization during Design Cycle – Architecture – Algorithm and System Levels – Power Optimization of Interconnects and Clocks – Dynamic Voltage Scaling – Clock Distribution – RTL power estimation and optimization – Model granularity – Model parameters – Model semantics – Model storage and Model construction – Power Optimization in Memories – Power in Cell Arrays – Power for Read and Write Accesses – Low Power Memory Technologies – Standby Power Optimization of Circuits and Systems – Power Optimization of Circuits and Systems during Operation – Low Power Design Methodologies and Flows – Power Characterization and Modeling – Low Power Clock – Data and Power Gating – Power Integrity.

TEXT BOOKS / REFERENCES:

1. Jan M. Rabaey, *Low Power Design Essentials*, Springer, 2009.
2. Christian Piguet, *Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools*, CRC Press, Taylor and Francis, 2006.
3. RakeshChadha and J. Bhaskar, *An ASIC Low Power Primer, Analysis, Techniques and Specification*, Springer,2013.
4. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, *Low power Methodology Manual for System on Chip*,Springer, 2007.

Outcomes:

- Understanding about various sources of power dissipation.
- Ability to estimate the power for given circuits.
- Ability to design low power digital VLSI circuits

16VL711 NETWORK ON CHIP 3-0-0-3

Objectives:

- To understand why there is a need for NoC.
- To learn about the various types of network architecture models available.

- To learn and understand the various issues present in interconnection links and various components used in NoC.
- To learn and understand the different types of switching, routing, addressing techniques and methods available for controlling the congestion and control flow in NoC.

Keywords: System on Chip(SoC), Network on Chip(NoC), Architecture, Topology, Signalling,Traffic patterns, Routers, Interconnection links, Switching, Routing, Addressing, Congestion control, Flow control, Network Interface.

Contents:

Introduction to NoC–NoCinSoCContext–OSI Layer Roles in Noc–Benefits and Challenges in Adapting NoCs–NoCModelingand Topology Exploration–Topology Exploration– Traffic Modeling and Topology Modeling–Interconnect Techniques– Interconnection in DSM SoC– High Performance Signaling and Low Power Interconnections –on –Chip Communication Reliability–Communication Architecture–Router Design– Switching Technique – Addressing and Routing Techniques –Congestion Control and Flow Control –NoCBased System Integration– NOC Interface Design and Clock Distribution –Power and Energy Savings in NoCs–Case Study on NoC Architecture for Mobile Application.

TEXT BOOKS / REFERENCES:

1. KonstantinosTatas, Kostas Siozios, DimitriosSoudris, Axel Jantsch,*Designing 2D and 3D Network on Chip Architecture*, Springer, 2013.
2. Glovanni De Micheliand Luca Benini, *Network on Chip: Technology & tools*, Morgan Kaufmann Publisher, 2006.
3. Axel Jantsch and HannuTenhunen, *Network on chip*,Kluwer Academy, 2003.
4. NicopoulosChrysostomos and Narayanan, *Network on Chip Architecture: A Holistic Design Exploration,Lecture Notes in Electrical Engineering*, Springer, 2009.

Outcomes:

- Ability to understand the need for NoC and the design an NoC architecture
- Ability to select a suitable traffic pattern for the analysis of the architecture depending upon the traffic load of a given application.
- Ability to select a suitable switching and routing techniques for the transmission of information from one node to another node satisfying the performance needs.
- Ability to handle the congestion and flow control problems which generally arises in an NoC architecture.

16VL712 WAVELETS AND APPLICATIONS 3-0-0-3

Objectives:

- To study the analysis, design and applications of filter banks and wavelets.
- To get hands-on Experience with Software.

Keywords: CWT, DWT, Legendre Polynomials, Multi Wavelets, EZW.

Contents:

Review of Fourier Theory – Heisenberg's Uncertainty Principle – Continuous Wavelet Transform (CWT) – Properties – Discrete Wavelet Transform (DWT) – Time-frequency Tiling – Short Time Fourier Transform – Wavelet and MRA – Vector Spaces – Scaling and Wavelet Functions – Filter Banks – Legendre Polynomials – Recurrence Formula – Laplace's Integral Formula – Design of Orthogonal Wavelet Systems – Bi-orthogonal Wavelet – Introduction to Lifting Scheme – Dealing with Signal Boundaries – Multi Wavelet – Frequency Domain Approach – Design of Wavelet – Wavelet in Image Processing – Biomedical Applications – Data Compression – EZW Algorithm – De-noising – Edge Detection – Object Isolation – Audio Coding – Communication Applications – Channel Coding – Speckle Removal – Image Fusion– MATLAB® Wavelet Toolbox – Software for Filter Design – Signal Analysis – Image Compression– PDEs –Wavelet Transforms on Complex Geometrical Shapes.

TEXT BOOKS / REFERENCES:

1. SomanK. P. andRamachandran K. I., *Insight into Wavelets from Theory to Practice*, Prentice Hall, 2004.
2. Rao R. M. and Ajith S. Bopardikar, *Wavelet Transforms - Introduction to Theory and Applications*, Pearson Education, 1999.
3. Howard L. Resnikoff and Raymond O. Wells, *Wavelets Analysis the Scalable Structure of Information*, Springer, 1998.
4. Strang G. and Nguyen T. Q., *Wavelets and Filter Banks*, Wellesley Cambridge Press, 1998.

Outcomes:

- Ability to use wavelets for non stationary signals.
- Ability to use wavelets for various applications including wave propagation, data compression, signal processing, image processing, pattern recognition, computer graphics.

16VL713 SEMICONDUCTOR MEMORY DESIGN 3-0-0-3

Objectives:

- To understand various semiconductor memory devices.
- To get an experience on how the memory related concepts are related to system design.
- To understand the packaging and reliability issues in memory modules.

Keywords: SRAM, DRAM, Memory Architecture, Reliability Analysis

Contents:

Random Access Memory Technologies – SRAM Cell Structures– MOS SRAM Architecture– MOS SRAM Cell and Circuit Operation– Advanced SRAM Architectures and Technologies– Application Specific SRAMs –CMOS– DRAM– DRAM Cell Theory – Cell Structures– Soft Error Failure in DRAM– EEPROM Technology – Architecture– Non-volatile SRAM– Flash Memories– Advanced Flash Memory Architecture – General Reliability Issues – RAM Failure Modes and Mechanism – Non-volatile Memory Reliability– Reliability Modeling and Failure Rate Prediction – Design for Reliability – Reliability Test Structures– Radiation Effects– Single

Event Phenomenon (SEP)– FRAMs– GaAs RAMs – Magneto Resistive RAMs (MRAMs)– Experimental Memory Devices– Memory Hybrids and MCMs (2D)– Memory Stacks and MCMs (3D)– Memory MCM Testing and Reliability Issues– Memory Cards– High Density Memory Packaging.

TEXT BOOKS / REFERENCES:

1. Ashok K. Sharma,*Semiconductor Memories: Technology, Testing, and Reliability*, Wiley, 2002.
2. Santosh K. Kurinec and Krzysztof Iniewski,*Nanoscale Semiconductor Memories: Technology and Applications*, CRC press, 2013.
3. Koichi Ishibashi and Kenichi Osada, *Low Power and Reliable SRAM Memory Cell and Array Design*, Springer, 2011.

Outcomes:

- Familiarity with the concepts of volatile and non volatile memories.
- Familiaritywith fault modelling issues in memory design.
- Familiaritywith stacking and packaging of memory modules.

16VL714 STATIC TIMING ANALYSIS 3-0-0-3

Objectives:

- To learn basic concepts of static timing analysis and apply them to constrain a design.
- Apply these concepts to set constraints, calculate slack values for different path types, identify timing problems.
- Analyze reports generated by static timing analysis tools.

Keywords: Timing Analysis Concepts, Timing Exceptions, Timing Violations, Noise-crosstalk glitch.

Contents:

Static Timing Analysis Concepts – Timing Exceptions– Timing Violations – Capacitance and Transition Violations – Temperature – Voltage – and Process –Timing–Clocks–Input / Output Timing –False Paths – Multi-Cycle Paths– Constraining Internal Reg-Reg Paths – Constraining I/O Interface Paths –Path Delay Calculation –Cell Delay – Net Delay –Delay Calculation with Interconnect –Slew Merging –Slack Calculation – Crosstalk and Noise–crosstalk Glitch Analysis–Crosstalk Delay Analysis Setup and Hold Analysis –Timing Verification– Synchronization – Synchronization Failure – Probability of Entering a Meta Stable State – Probability of Staying in the Meta stable State–multi-cycle Paths–False Paths–Timing Across Clock Domains– Clock Network Optimization –Clock Skew– Scheduling – Clock Distribution Problem– Off-Chip Clock Distribution – Clock Trimming – On-Chip Clock Distribution– On-Chip Clock Tree – Reducing Jitter– Pre-Layout Clock Specification – Post-Layout Clock Specification –Parallel Timing Optimization –Circuit Partitioning for Independent Timing Regions – Post-Silicon Timing Validation–Post-Silicon Tuning – on-chip Variations –Time Borrowing–Clock Gating Checks – sign-off Methodology–Statistical Static Timing Analysis.

TEXT BOOKS / REFERENCES:

1. J. Bhasker, R. andChadha,*Static Timing Analysis for Nanometer Designs: A Practical Approach*, Springer, 2009.
2. William J. Dally and John W. Poulton, *Digital Systems Engineering* Cambridge University Press, 2008.
3. Charles J. Alpert Dinesh P., Mehta SachinandS. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, CRC Press, 2009
4. Stephen H. Hall and Howard L. Heck, *Advanced Signal Integrity forHigh-speed Digital Designs*, John Wiley Publication, 2009.

Outcomes:

- Ability to identify and apply timing arc information from a library.
- Ability to use wire-load information to calculate net delays.
- Ability to identify the properties of a clock, including period, edges, slew, and duty cycle.
- Ability to apply setup and hold checks to diagnose design violations.

16VL715 OPTOELECTRONIC DEVICES 3-0-0-3

Objectives:

- To learn the concepts and applications of optoelectronic devices.
- To study the optoelectronic devices required to build optical transmitter and receiver for optical communication.

Keywords: Semiconductor, Crystal Structures, Hetero Structures, Optical Properties, Lasers.

Contents:

Optical Properties in Semiconductor–Direct and Indirect Band-Gap Materials –Radiativeand Non-Radiative Recombination – Optical Absorption –Photo-Generated Excess Carriers – Minority Carrier Life Time– Luminescence and Quantum Efficiency in Radiation–Light Emitting Diode (LED) –Materials for Visible and Infrared LED– Structure and Coupling to Optical Fibers –Stimulated Emission and Light Amplification –Spontaneous and Stimulated Emission–Einstein Relations– Population Inversion – Absorption of Radiation – Optical Feedback and Threshold Conditions–Semiconductor Lasers– Operating Wavelength– Threshold Current Density–Hetero-Junction Lasers– Optical and Electrical Confinement– Band Offsets and Hetero Structure Types–Optical Properties of Quantum Structures–Photo-Detectors– Photoconductors–PIN Detectors– Avalanche Photodiodes and Phototransistors–Noise in Photo Detectors–Photo Detector Design Issues – Silicon and SchottkySolar Cells –Quantum Dot Infrared–Optical Modulators– Electro-Optic Effect– Acousto-Optic Effect and Magneto-Optic Devices– Quantum-Confined Stark Effect–Introduction to Photo Receiver Systems– Performances like SNR– Sensitivity and Noise –Monolithic Photo Receiver.

TEXT BOOKS / REFERENCES:

1. Pallab Bhattacharya, *Semiconductor Optoelectronic Devices*, Second Edition, Prentice Hall of India, Reprint 2011.

2. S.O. Kasap, *Optoelectronics and Photonics: Principles and Practices*, Second Edition, Prentice Hall, 2012.
3. Govind P. Agrawal, *Fiber-Optic Communication Systems*, Third Edition, John Wiley and Sons, Reprint 2007.
4. Wilson J and Hawkes J. F. B, *Optoelectronics: An Introduction*, Second Edition, Prentice-Hall, 1992.

Outcomes:

- Ability to do research on optoelectronic devices such as photo detectors.
- Familiarization with the concepts of quantum effect optoelectronic devices.

16VL716 VLSI FABRICATION TECHNOLOGY 3-0-0-3

Objectives:

- To understand the scientific principles involved in the fabrication process.
- To introduce the concept of clean rooms and understand the challenges and limitations involved in extending each fabrication process into the nano-era.
- To introduce some new fabrication concepts employed in industry recently.

Keywords:IC Fabrication, Silicon Processing, Crystal Growth, Photo Lithography, Oxidation, Diffusion, Etching, Copper Interconnects, CMOS Technology, Film Deposition

Contents:

Process Overview – Crystal Growth, Wafer Fabrication, and Basic Properties of Silicon Wafers – Clean Rooms and Wafer Cleaning – Lithography – Light sources, Exposure systems, Resists, Masks – Steps in practical Lithography – Advanced Mask Engineering - Non-optical Lithographic Techniques – DopantDiffusion – Thermal Oxidation – Oxide growth models – Oxide Characterization – Alternative Gate Dielectrics – Etching – Wet , Plasma, Ion Milling – Reactive Ion Etching – Ion Implantation – Methods and Models – Thin film Deposition – Physical, Chemical and Epitaxial methods – Process Integration – Back End Technology – Device Isolation – Contacts and Metallization – Silicon Integrated Circuit Process Sequences – CMOS Process – Bipolar Process – MEMS Fabrication.

TEXT BOOKS / REFERENCES:

1. Stephen A. Campbell, *Fabrication Engineering at the Micro- and Nanoscale*, Fourth Edition, Oxford University Press, 2013
2. Peter Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, Sixth Edition, McGraw-Hill Professional, 2014.
3. James D. Plummer, Michael D. Deal and Peter B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*, Prentice Hall (Indian edition published by Dorling Kindersly India Pvt. Ltd), New Delhi, 2001.
4. Richard C. Jaegar, *Introduction to Microelectronic Fabrication: Volume 5 of Modular Series on Solid State Devices*, Second Edition, Prentice Hall, 2002.

Outcomes:

- Familiarization with Silicon processing and IC fabrication.

- Clarity on the constraints and modifications needed in extending these processes to nano-era.
- Familiarization with some of the latest techniques used in semiconductor industry.

16VL717 PHYSICAL DESIGN OF INTEGRATED CIRCUITS 3-0-0-3

Objectives:

- To develop algorithms for placement and power routing.
- To analyze the setup and hold times in physical domain.
- To decrease the timing cost by adopting new routing techniques.

Keywords: Placement, Timing Analysis, Power Planning, Multivoltage, Clock Tree Synthesis, Routing,RC Extraction

Contents:

Physical IC Design–Objectives–VLSI Physical Design Cycle–Circuit Layout–Partitioning–Floor Planning–Placement–Specific Floor Planning Problems–Power Density Map–Advanced Low-Power Floor Planning–Multi-Voltage PG Routing–Floor Planning for Low PowerTiming Analysis &Optimization–Basic Timing Checks–Timing Constraints(SDC) – Timing Corners–Timing Report Analysis–Crosstalk and Noise –Clock Distribution Networks–Clock Tree Synthesis–Clock Skew–Clock Power– Area-Congestion Map–Clock Tree Optimization–High Fan-Out Synthesis (HFS)–Routing Steps in Physical Synthesis–Classification of Routing Methods–Grid-Based Routing System–Global Routing–Top-Level Congestion–Detailed Routing–Channel Routing Problem–Analysis and Optimization Types–Best/Worst Analysis – Combination of Corners and Modes–Parasitic Extraction (RC Extraction)–Chip Finishing Overview–Antenna Fixing–Parasitic (SPEF or SBPF)–Final Validation– Net List Output–GDS2 Output–Basic FPGA Architecture–Technology Mapping for FPGA - FPGA Routing Algorithm.

TEXT BOOKS / REFERENCES:

1. K. Golshan, *Physical Design Essentials: An ASIC Design Implementation Perspective*, Springer, 2010
2. J.P. Uyemura, *Modern VLSI Design – System-on-Chip Design*, Prentice-Hall, 2002
3. A. B. Kahng,*VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer, 2011
4. Stephen D. Brown, Robert J. Francis, Jonathan Rose andZvonko G. Vranesic, *Field-Programmable Gate Arrays*, Springer, 2012.

Outcomes:

- Familiarize with the latest techniques adopted in physical domain.
- Familiarize with the concepts of timing violation and fixing.

16VL718 MIXED SIGNAL VLSI DESIGN 3-0-0-3

Objectives:

- To give an insight in to the design and analysis of mixed circuit design.
- To introduce Verilog AMS and to provide a platform for doing basic blocks with Verilog-A.

Keywords: Discrete time, sample and hold, filters, ADC, DAC, PLL.

Contents:

Continuous Time Signals – Discrete Time Signals – Laplace Transform – Z Transform – Sample and Hold Circuit – Analog Continuous Time Filters –Passive and Active Filters –Switched Capacitor Filters– Basic Building Blocks – Analysis and Non-Idealities–Introduction to VerilogA – Ideal D/A and A/D Converters – Quantization Noise – NyquistRateA/D Converters – Comparators Characterization – Two Stage Comparators –Flash Converter and Successive Approximation Converters –Oversampling Converters – Without and with Noise Shaping – Analog Multiplier Design – Simple PLL –Mixed Signal Current Mode and Voltage Mode DC – DC Converters –Layout Techniques for Basic Mixed Signal Blocks.

TEXT BOOKS / REFERENCES:

1. BehzadRazavi, *Principles of Data Conversion System Design*, John Wiley and Sons,1995.
2. BehzadRazavi, *Design of Analog Integrated Circuits*,McGraw-Hill, 2001.
3. Kenneth S. Kundart and Olaf Zinke,*The Designer's Guide to Verilog - AMS*, Springer,2004.

Outcomes:

- Familiarization of advanced topics in Analog and Mixed Circuit Design.
- Familiarization of the working of data converters.
- Ability to model and verify with Verilog - A.

16VL719 COMMUNICATION SYSTEMS AND NETWORKS 3-0-0-3

Objectives:

- To study the basics of sampling and quantization, coding, modulation, signal detection and system performance in the presence of noise.
- To study the data networking concepts including multiple access, reliable packet transmission, routing and protocols of the internet.

Keywords: Digital Modulations, Signal Detection, Multiple Access, Routing Protocols
Contents:

Review of Digital Communication Systems – Sampling – Quantization –Waveform Coding Formats – Pulse Shaping and Matched Filter – Baseband Modulation Techniques– MPSK, MQAM– Pass Band Modulation Techniques – QAM – Performance of Digital Modulation – AWGN Channels – Fading Channels – Capacity in AWGN Channels and Fading Channels – ErgodicCapacity and Outage Capacity – Multi user Systems– Sum Rate Capacity– Multiple Access Techniques – TDMA, FDMA, SDMA, CDMA, OFDMA – Interference Limited Systems – Noise Limited Systems– Case Studies and Design Applications.

TEXT BOOKS / REFERENCES:

1. John Proakis and MasoudSalehi,*Digital Communications* , Fifth Edition, McGraw-Hill Publications, 2007.
2. Simon S Haykins, *Digital Communication Systems*, Wiley Publication, 2013.
3. David Tse and PramodVishwanath, *Fundamentals of Wireless Communication*, Cambridge University Press, 2005.
4. Ray Horak, *Communications Systems and Networks*, Third Edition, Wiley Inc., 2002

Outcomes:

- Ability to design a communication system with specific high level constraints.
- Ability to apply the concepts in the context of aerospace communication systems: aircraft communications, satellite communications, and deep space communications.
- Ability to evaluate and assess the performance of communication networks in real time setting.

16VL720 OPTIMIZATION METHODS 3-0-0-3

Objectives:

- To provide a platform to explore basic optimization algorithms.
- To demonstrate the suitability of different algorithms for different demands in applications.

Keywords: Graph, Cycles, Trees, Edges, Vertex, Coloring, Objective Functions, Constraints.

Contents:

Introduction to Optimization Methods –Problem Formulation – Single Variable and Multi-Variable Optimization with Equality and Inequality Constraints – Lagrange Multiplier Method – KKT Method –Linear Programming –Graphical Methods –Simplex Method – Duality Method – Duality Simplex Method –Sensitivity Analysis –Non-Linear Programming –Direct Search Methods –Gradient Methods –Steepest Descent Methods – Quasi-Newton Method –Dynamic Programming –Calculus Method – Tabular Method.

TEXT BOOKS / REFERENCES:

1. K. Deb, *Optimization for Engineering Design – Algorithms and Examples*, Printice Hall, 1995.
2. S. S. Rao, *Engineering Optimization Theory and Practices*, *New Age International(P) Ltd., 2000*.

Outcomes:

- Ability to formulate the optimization problems.
- Ability to choose the best optimization algorithm for given problems.

16VL721 ELECTRONIC PACKAGING AND RELIABILITY 3-0-0-3

Objectives:

- To introduce basic concepts and types in Microchip Packaging.
- To understand how packaging needs vary for various applications
- To understand the thermal, mechanical, electrical and chemical degradation mechanisms that affect the reliability of packages.

Keywords:IC Fabrication, Silicon Processing, Crystal Growth, Photo Lithography, Oxidation, Diffusion, Etching, Copper Interconnects, CMOS Technology, Film Deposition

Contents:

General Packaging Principles –Wire Bonding – Flip Chip Technologies –Types of Packaging – Ball Grid Array – Quad Lead – Surface Mount Technology –Component Packaging (Including Integrated Circuits, Opto, MEMS, RF and Solar Devices) –Substrates used in Packaging – Electrical and Thermal Considerations –Reliability Test Strategies –Reliability Modelling – Degradation and Failure Mechanisms – Thermal – Chemical – Electrical and Mechanical – Characterization Techniques.

TEXT BOOKS / REFERENCES:

1. Andrea Chen and Randy Hsiao-Yu Lo, *Semiconductor Packaging: Materials Interaction and Reliability*, CRC Press, 2012
2. Peter Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, Sixth Edition, McGraw-Hill Professional, 2014.
3. Richard K. Ulrich and William D. Brown,*Advanced ElectronicPackaging*, John Wiley & Sons, Inc., 2006.
4. Richard C. Jaegar, *Introduction to Microelectronic Fabrication***:** *Volume 5 of Modular Series on Solid State Devices*, Second Edition, Prentice Hall, 2002.

Outcomes:

- Exposure to various IC packaging techniques.
- Understanding the constraints in each techniques and modifications needed in extending these to various applications
- Understanding of the reliability issues in packaging.

16VL722MEMS DESIGN AND FABRICATION 3-0-0-3

Objectives:

- Understanding the basics of Micro Electro Mechanical Systems and the processing technologies
- To understand the concepts and principles of micro sensors, actuators and their fabrication techniques
- Understand the applications of MEMS in various fields

Keywords: Microelctronic Technologies, Smart Materials Systems, Micromachining

Contents

Introduction to MEMS – MEMS materials – Standard Microelctronic Technologies- Silicon and Polymeric MEMs Fabrication – MEMS and Smart Materials Systems – Silicon Bulk Micromachining - Silicon Surface Micromachining - Microsensors and Microactuators – Fabrication and Packaging of Smart Microsystems – MEMS based Sensors and Devices for Satellite Communication – Space Technology – Medical and Aerospace Applications – Wireless Technology – Smart Sensors and MEMS Devices.

TEXT BOOKS/REFERENCES:

1. Julian W. Gardner, Vijay K.Varadan and Osama O. Awadelkarim, "*Microsensors, MEMS, and Smart Devices",* Wiley, 2001.
2. Jha A. R., "*MEMS and Nano Technology – Based Sensors and Devices for Communications Medical and Aerospace Applications",* CRC press, 2008.
3. Vijay K. Varadan, Vinoy K.J. and Gopalakrishnan S., "*Smart Material Systems and MEMS: Design and Development Methodologies",* Wiley, 2006.
4. Richard Zurawsky, "*Embedded Systems Handbook",* CRC Press, 2006.
5. Steven S. Saliterman, "*Fundamentals of BioMEMS and Medical Microdevices",* SPIE Press, 2006.

Outcome:

- Able to understand the concept of MEMS based systems and devices
- Able to understand the applications of MEMS in satellite, space technology, medical and aerospace.

16VL723 EMERGING ARCHITECTURES FOR MACHINE LEARNING 3-0-0-3

Objectives:

- To introduce new paradigms in computing.
- To get an exposure to popular Cloud and IoT technologies.
- To introduce the potential of FPGAs in neural networks and bioinformatics.
- Provide hands on exposure in designing systems using state of the art computing tools.

Keywords: GPU, CUDA, Cloud and IoT, Machine Learning.

Contents:

Accelerated Computing – GPUs – Overview of GPU Architectures – CUDA – OpenCL – Case Studies IoT and Cloud Architectures – Use Cases – VLSI Design Challenges for IoT– Power – Area and Security – Intel Dashboard Framework – Overview of Cloud Computing – Introduction to Hadoop Framework – Case Study – FPGA Architectures for Neural Networks and Bioinformatics – Review of Neural Networks – Data Precision and Implementation Issues – Case Studies of Regression Implementation – FPGA and Reconfigurable Architectures for Bioinformatics – Database Search – Sequencing and Alignment

TEXT BOOKS / REFERENCES:

1. David B. Kirk, Wen-Mei W. Hwu, *Programming Massively Parallel Processors: A Hands-on Approach*, Second Edition, Morgan Kauffman
2. Bertil Schmidt, *Bioinformatics: High Performance Parallel Computer Architectures*, CRC Press, 2011
3. Amos R Omondi and Jagath C Rajapakse, *FPGA Implementation of Neural Networks*, Springer 2006.
4. ArshdeepBahga and Vijay Madisetti, *Internet of Things A Hands on Approach*, Published by the Authors, 2014

Outcomes:

- Ability to design neural network and high performance bioinformatic database analysis systems.
- Ability to design solution for solving problems in a Big Data Cloud Environment.
- Ability to suggest GPU based solutions for dataflow intensive problems.
- Ability to use IoT technologies to design efficient applications.