Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Very Large Scale Integrated (VLSI) Circuit Design is setting the benchmark for the growth of technology. M. Tech in VLSI Design addresses the state-of-the-art design technology using computer-aided design (CAD) tools and associated hardware. The course demands learning the principles of VLSI design and fabrication, understanding the complete design flow and developing expertise to design CMOS chips for industrial requirements. The programme lays the foundation for career opportunities in leading VLSI design industries, research labs, and reputed national and international organizations.

The salient features of the programme include:

- Experienced domain-specific faculty
- Excellent infrastructure with fully equipped laboratories
- Seminars / Expert lectures / Webinars
- Student publications
- Integrated M.Tech + PhD Programmes
- International Program Opportunities
- Placements and Internships

Students are exposed to various design software tools in this programme. Also, they learn to design, simulate, implement and test complex digital systems using FPGAs (Field Programmable Gate Arrays). Students are trained in several topics that cut across different domains, starting from the lowermost level of physical devices to the top level of application development. Expertise across different domains of VLSI design flow such as VLSI architecture & design, testing and verification, and device technology is a major highlight of the programme. Current focus areas include hardware security, VLSI architectures for signal processing, CAD for VLSI, high frequency CMOS design and modelling, device modelling for nano electronics, low power VLSI and timing analysis. Ample scope exists for pursuing interdisciplinary research through collaboration and exchange programmes with various national and international institutions.

Programme Educational Objectives (PEOs)

PEO1	To create manpower in VLSI domain so as to attain mastery in applying VLSI concepts to engineering problems in electronics, communication and computing so as to meet the need of the industry, teaching, higher education or research.
PEO2	Creation of state-of-the-art expertise in the microelectronics domain to deal with design, development, analysis, testing and evaluation of the critical aspects of integrated circuits and its core concepts.
PEO3	To exhibit professional competence and leadership qualities with harmonious blend of ethics leading to an integrated personality development.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Programme Outcomes (POs)

PO1	An ability to independently carry out research /investigation and development work to solve practical problems.
PO2	An ability to write and present a substantial technical report/document.
PO3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program.
PO4	An ability to use modern tools for engineering design problems, analyze the performance and optimize the systems-level approaches.
PO5	An ability to engage in independent and life-long learning in the context of technological change and industrial demands.

Semester – I

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
FC	21VL601	Embedded Computing and Programming	3	0	0	3
FC	21VL602	Machine Learning and Algorithm Design	3	0	0	3
SC	21VL611	CMOS Digital Integrated Circuits	3	0	0	3
SC	21VL612	Digital Circuits and Systems	3	0	0	3
SC	21VL613	Analog VLSI Circuits	3	0	0	3
SC	21VL681	Machine Learning and Embedded Programming Lab	0	0	4	2
SC	21VL682	Front End Simulation and FPGA Synthesis Lab	0	0	4	2
HU	21HU601	Amrita Value Program				P/F
HU	21HU602	Career Competency- I				P/F
		Total	15	0	8	19

Semester – II

Type	Code	Course Name	Teaching Schemes	Credits

			L	T	P	
SC	21VL614	Functional Verification with Hardware Description Languages	3	0	0	3
SC	21VL615	Digital VLSI Testing & Testability	3	0	0	3
E		Elective I	3	0	0	3
E		Elective II	3	0	0	3
E		Elective III	3	0	0	3
SC	21VL683	ASIC Design and FPGA Lab	0	0	4	2
SC	21VL684	Functional Verification Lab	0	0	4	2
SC	21RM613	Research Methodology	2	0	0	2
HU	21HU603	Career Competency – II	0	0	2	1
		Total	17	0	10	22

Semester – III

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
E		Open Elective *	3	0	0	3
SC	21LIV604*	Open Lab/Live-in Lab	0	0	4	2
P	21VL798	Dissertation- Phase I	0	0	20	10
		Total	3	0	24	15

*This can be either regular courses on campus or online portal based with prior approval.

*** 21LIV604-Code for Live-in-Lab**

Semester – IV

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
P	21VL799	Dissertation – Phase II	0	0	28	14
		Total	0	0	28	14

Total Credits: 70

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Program Specific Elective Courses

Domain Name: Circuits and Technology

Sl.No	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
1	21VL701	Semiconductor Device Modelling	3	0	0	3
2	21VL702	VLSI Fabrication	3	0	0	3
3	21VL703	VLSI Data Conversion Circuits	3	0	0	3
4	21VL704	Semiconductor Memory Design	3	0	0	3
5	21VL705	Mixed Signal VLSI Design	3	0	0	3
6	21VL706	CMOS RF IC Design	3	0	0	3
7	21VL707	VLSI Signal Conditioning	3	0	0	3
8	21VL708	Optoelectronic Devices	3	0	0	3

Domain Name: Design, Test and Verification

Sl.No	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
1	21VL711	Application Specific Integrated Circuits	3	0	0	3
2	21VL712	Low Power VLSI Circuit Design	3	0	0	3
3	21VL713	FPGA based System Design	3	0	0	3
4	21VL714	Electronic System Level Design	3	0	0	3
5	21VL715	System-on-Chip & FPGA Testing	3	0	0	3

Domain Name: Computational VLSI

Sl.No	Code	Course Name	Teaching Schemes	Credits

			L	T	P	
1	21VL721	VLSI Architectures for Multicore and Heterogeneous Computing	3	0	0	3
2	21VL722	Emerging Architectures for Machine Learning	3	0	0	3
3	21VL723	Wavelets and Applications	3	0	0	3
4	21VL724	Data Structures and Algorithms	3	0	0	3
5	21VL725	Reconfigurable Computing	3	0	0	3
6	21VL726	VLSI Signal Processing	3	0	0	3
7	21VL727	Static Timing Analysis	3	0	0	3
8	21VL728	Computer Aided Design for VLSI Circuits	3	0	0	3

Domain Name: Systems and Security

Sl.No	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
1	21VL731	Cryptography	3	0	0	3
2	21VL732	Network on Chip	3	0	0	3
3	21VL733	Hardware Software Co-Design	3	0	0	3
4	21VL734	Hardware Security and Trust	3	0	0	3
5	21VL735	VLSI IoT	3	0	0	3

21VL601 Embedded Computing and Programming 3-0-0-3

Learning Objectives

LO1 To introduce design concepts of embedded systems.

LO2 To provide insights on embedded C programming for configuring microcontroller and peripherals.

LO3 To enable development of embedded system models.

Course Outcomes

CO1 Ability to identify the features of STM32F microcontroller.

CO2 Ability to apply embedded C programming skills for configuring STM32F peripherals.

CO3 Ability to analyze external peripheral interfacing with a microcontroller.

CO4 Ability to design and develop embedded systems using STM32F microcontroller. CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	-
CO 2	-	-	2	3	2
CO 3	-	-	2	3	2
CO 4	-	-	2	3	3

Skills Acquired: Provide detailed insight on configuration and programming of various peripherals in STM32 Microcontroller.

Course Contents

Unit 1: (15 hours)

STM32F Processor - Introduction to Embedded Systems - Introduction to ARM - Advanced RISC Features - Core Data Path - Register Organization - System Architecture - Memory Organization - Low Power Modes - Power Control Registers - Backup Registers - Programming STM32F.

Unit 2: (15 hours)

STM32F Peripherals - Introduction to Embedded C Programming - General Purpose Input Output - UART - ADC - DAC - Timers - Interrupts and Exceptions - PWM - SPI.

Unit 3: (15 hours)

External Peripheral Interfacing - LCD - Keypad - Motor - Servo Motor - EEPROM - Seven Segment Interfacing - Sensor Interfacing.

References

1. Muhammad Ali Mazidi, *STM32 Arm Programming for Embedded Systems*, 2019.
2. Donald Norris, *Programming with STM32: Getting Started with the Nucleo Board and C/C++*, McGraw-Hill Education, 2018.
3. *STM32F446xx Advanced Arm®-based 32-bit MCUs, Reference Manual*, 2020.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design
21VL602 Machine Learning and Algorithm Design 3-0-0-3

Learning Objectives

LO1 To introduce the concepts and provide a mathematical foundation for developing machine learning models.

LO2 To provide insights on the evaluation of machine learning models for various applications.

LO3 To impart knowledge on algorithm design and its applications.

Course Outcomes

CO1 Ability to understand concepts of machine learning and algorithm design.

CO2 Ability to apply machine learning and algorithm design concepts for analysis of problems.

CO3 Ability to analyze and process datasets using machine learning techniques for extracting useful information.

CO4 Ability to design and implement machine learning models for the given task.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	-
CO 2	-	-	2	3	2
CO 3	-	-	2	3	2
CO 4	-	-	2	3	3

Skills Acquired: The design and programming ability in machine learning model development for a wide range of industrial applications.

Course Contents

Unit 1: (15 hours)

Mathematical Concepts Review - Central Tendency - Dispersion of Data - Descriptive Data Summaries - K-Nearest Neighbors Classifier - Bayes Classifiers - Classifier Performance Measures.

Unit 2: (15 hours)

Decision Tree - Ensemble Methods - Ordinary Least Squares - Artificial Neurons - Perceptron - Multi Layer Perceptron and Back Propagation - Hyperparameter Tuning - Cluster Analysis - Partitioning Methods - Hierarchical Methods - Density-Based Methods - Cluster Evaluation.

Unit 3: (15 hours)

Graphs - Definitions and Applications - Graph Connectivity - Graph Traversal - Testing Bipartiteness - Breadth - First Search - Directed Graphs - Directed Acyclic Graphs Topological Ordering - Interval Scheduling - Optimal Caching - Shortest Paths - Minimum Spanning Tree - Clustering - Huffman Codes - Data Compression - Partitioning Problems - Graph Coloring.

References

1. Jiawei Han, Micheline Kamber, Jian Pei, *Data Mining: Concepts and Techniques*, Third Edition, Morgan Kaufmann Publishers (Elsevier), 2011.

2. Aurélien Géron, *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems,* Second Edition, O'Reilly Media, 2019.
3. Earl Gose, Richard Johnson Baugh, Steve Jost, *Pattern Recognition and Image Analysis,* Pearson Education India, 2015.
4. Jon Kleinberg, ÉvaTardos, *Algorithm Design*, Pearson, 2006.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

CMOS Digital Integrated Circuits

21VL611 **3-0-0-3**

Learning Objectives

LO1 To introduce the concept of MOS and CMOS logic styles.
LO2 To comprehend the design of transistor level digital circuits.
LO3 To enable learning different logical implementation.
LO4 To impart knowledge on switch level RC delay models.

Course Outcomes

CO1 Ability to understand/visualize the digital logic functions at device level.
CO2 Ability to apply suitable CMOS logical styles for the given application.
CO3 Ability to analyze the architecture and characterization of combinational circuits. CO4 Ability to design digital CMOS circuits and measure delay performance.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	2
CO 2	-	-	2	2	2
CO 3	-	-	3	3	3
CO4	-	-	3	3	3

Skills Acquired: Design of CMOS logic circuits and performance analysis of digital architectures.

Course Contents

Unit 1: (15 hours)

VLSI design flow - NMOS and PMOS Transistors– CMOS Fabrication and Layout - Threshold Voltage - MOS Transistor Theory - I-V and C-V Characteristics - Second-Order Effects - NMOS and CMOS Inverters - Inverter Ratio - CMOS Combinational Logic Gates - Multiplexers.

Unit 2: (15 hours)

CMOS Transistor Characteristics - Delay Time Estimation - Switching Characteristics - CMOS Logic Structures - PTL - CPL - Pseudo logic - Transmission Gates – Static CMOS Design - Dynamic CMOS Design - RLC Estimation - Elmore's Delay Model.

Unit 3: (15 hours)

Transistor Sizing – Power Dissipation and Design Margin - Charge Sharing - Logical Effort - Scaling - Combinational Circuits - Interconnects - Electro Static Discharge (ESD) - LatchUp and Prevention - Sequential Circuit Design - Timing Analysis.

References

1. Jan M. Rabaey, Anantha P. Chandrakasan and Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, Second Edition, Prentice Hall India, 2003.
2. Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits - Analysis and Design*, Third Edition, Tata McGraw-Hill, 2003.
3. Neil H. E. Weste and David Money Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison Wesley, 2010

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

21VL612 **Digital Circuits and Systems** 3-0-0-3

Learning Objectives

LO1 To understand HDL Based Digital Design flow at RTL abstraction.
LO2 To introduce HDL modeling of combinational and sequential building blocks.
LO3 To introduce design of different subsystems using HDL design flow.

Course Outcomes

CO1 Ability to understand the effect of modeling styles on synthesis of hardware.
CO2 Ability to design a system at the RTL abstraction.
CO3 Ability to develop models for combinational and sequential blocks.
CO4 Ability to model and evaluate architectures for digital systems.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	3	-
CO 3	-	-	3	3	-
CO4	-	-	3	3	3

Skills Acquired: Design of the architecture of a system for a given specification at RTL abstraction and modeling the architecture in HDL.

Course Contents

Unit 1: (15 hours)

Introduction to VLSI Design Flow - RTL Abstraction - Different Modeling Styles in Verilog - Design of Combinational Subsystems.

Unit 2: (15 hours)

Sequential Building Blocks - Flip-flops – Registers - Shift Registers and Counters - State Machines - Basic Aspects of Timing - Digital Subsystem Design - FIFOs - Memories - Buffers - DSP Building blocks - Wordlength Effects - Fixed - Floating Point Representation.

Unit.3: (15 hours)

Case Study of Design and Modeling of a Simple Digital System - Datapath and Controller Design - Programmable Logic Devices - CPLD - FPGA - Verilog Design for FPGA Synthesis - Block RAMs – Introduction to High Level Synthesis.

References

1. Michael D. Ciletti, *Advanced Digital Design with Verilog HDL*, Second Edition, Pearson Higher Education, 2011.
2. Morris Mano and Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, Fifth Edition, Pearson Higher Education, 2013.
3. Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, Third Edition, McGraw Hill, 2014.
4. Peter Minns and Lan Elliott, *FSMBased Digital Design Using Verilog HDL*, Fifth Edition, John Wiley and Sons Ltd, 2008.
5. Wayne Wolf, *FPGA Based System Design*, Pearson Ltd., 2004.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

21VL613 Analog VLSI Circuits 3-0-0-3

Learning Objectives

LO1 To provide an overview of MOS characteristics and its importance in analog design.

LO2 To introduce the design and analysis of active loaded amplifiers with and without feedback.

LO3 To provide a practical approach for design of operational amplifiers.

Course Outcomes

CO1 Ability to understand MOS characteristics and the design of current sources.

CO2 Ability to apply techniques to design actively loaded amplifiers with and without feedback.

CO3 Ability to design and analyze operational amplifiers, comparators and oscillators.

CO4 Ability to evaluate amplifier characteristics from top-level specifications using circuit simulators.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	-
CO 2	-	-	3	-	-
CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired: Provides a platform to design CMOS amplifiers with the help of industry standard tools.

Course Contents

Unit 1: (15 hours)

MOS Large-Signal and Small-Signal Equivalents - Biasing - High-Frequency Modeling - Short Channel - Subthreshold Operation - Leakage Current - MOS Diodes - Active Resistors - Capacitors - Current Sink and Source - Cascode Current Mirrors - Gain-Boosting – Current and Voltage References - Supply Independent Biasing – Sensitivity.

Unit 2: (15 hours)

MOS Inverters - Active Load - Current Source Load - Push-Pull Load - Small Signal Gain - Frequency Response - Miller Effect-3-dB Frequency Determination - Single-Stage MOS Amplifiers - Common Gate - Common Drain - Cascode - Differential Amplifiers - Active Loaded Differential Pair - Feedback Amplifiers - Negative Feedback - Loop Gain - Oscillators – Comparators.

Unit 3: (15 hours)

Two-Stage CMOS Op-Amp Design - Gain and Frequency Response - Stability and Compensation in CMOS Op-Amps - Miller Compensated Op-Amp - Lead-Lag Compensation - Case Study of ADA4528: A Zero Drift and Ultralow Noise Op-Amp.

References

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill, 2002, Reprint 2015.
2. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Third Edition, Oxford Press, 2011.
3. P. R. Gray, P. J. Hurst, S. H. Levis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Fifth Edition, Wiley Student Edition, 2009.
4. A S. Sedra, K. C. Smith and A. N. Chandorkar, *Microelectronic Circuits -Theory and Applications*, Seventh Edition, Oxford University Press, 2017.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

21VL681 Machine Learning and Embedded Programming Lab 0-0-4-2

Learning Objectives

LO1 To provide design concepts on implementation of Embedded Systems.
LO2 To provide insight on communication protocols used in embedded domain.
LO3 To demonstrate peripheral configuration of a microcontroller platform.
LO4 To provide insights into design and implementation of machine learning algorithms.

Course Outcomes

CO1 Ability to interface external peripherals with a programmable platform.
CO2 Ability to implement and analyze serial communication protocol.
CO3 Ability to design and implement embedded system or machine learning based solutions for a specific application.
CO4 Ability to analyze and optimize the performance of the given machine learning model.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	2	-	2	3	2
CO 2	2	-	2	3	2
CO 3	3	3	3	3	3
CO 4	3	3	2	3	3

Skills Acquired: Programming ability in embedded system design and machine learning model development for a wide range of applications.

Lab Course Contents

Ex.No	Experiment details
1	General Purpose Input Output Configuration and Programming
2	LCD and Keypad Interfacing
3	Universal Asynchronous Receiver and Transmitter (UART) Configuration and Programming
4	Analog to Digital Convertor (ADC) Peripheral Configuration and Programming
5	Timer Configuration and Programming
6	PWM Generation and Motor Speed Control
7	Design and Implementation of a Bayes Classifier for Two-Class and Multi-Class Classification
8	Design and Implementation of an MLP Based Artificial Neural Network Model for Classification or Regression
9	Design and Implementation of a Deep Learning Classifier Model Using Transfer Learning
10	Design and Implementation of a Simple DAG Network for Deep Learning
11	Design and Implementation of Clustering Algorithms
12	Determining the Bipartiteness of a Graph Using Search Algorithms

Recommended Tools

STM32CubeMX, Keil µVision, MATLAB, Python

References

1. Muhammad Ali Mazidi, *STM32 Arm Programming for Embedded Systems*, 2019.
2. Donald Norris, *Programming with STM32: Getting Started with the Nucleo Board and C/C++*, McGraw-Hill Education, 2018.
3. *STM32F446xx advanced Arm®-based 32-bit MCUs, Reference Manual*, 2020.
4. Aurélien Géron, *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems*, 2nd Edition, O'Reilly Media, 2019.

Evaluation Pattern

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Based on Lab Experiments, and Term Work with Report.

21VL682 Front End Simulation and FPGA Synthesis Lab 0-0-4-2

Learning Objectives

LO1 To introduce HDL modeling and simulation at RTL abstraction of combinational and sequential subsystems.

LO2 To provide understanding of writing proper test benches.

LO3 To provide exposure to different HDL modeling styles and their applications. LO4 To instill background in assessing the impact of coding styles on synthesis.

Course Outcomes

CO1 Ability to understand modeling styles.
CO2 Ability to apply modeling styles for realizing digital subsystems.
CO3 Ability to verify and analyze HDL models by writing appropriate test benches.
CO4 Ability to evaluate the impact of coding styles on synthesis.
CO5 Ability to develop RTL architectures for simple digital systems.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	3	-
CO 3	-	-	3	3	-
CO4	-	-	3	3	-
CO5	2	-	3	3	3

Skills Acquired: Build basic designs and incorporate them into system level design and to do experiments using FPGA and other tools for various digital designs.

Lab Course Contents

Ex.No	Experiment details
1	Introduction to HDL Simulation Flow
2	Structural and Dataflow Modeling in Verilog
3	Behavioral Modeling and Verification of Combinational Subsystems
4	Behavioral Modeling, Synthesis and FPGA implementation of Combinational Subsystems
5	Behavioral Modeling and Verification of Flip-Flops, Registers and Counters
6	Behavioral Modeling and Verification of Finite State Machines
7	Behavioral Modeling, Synthesis and FPGA implementation of Flip-flops, Registers and Counters
8	Behavioral Modeling, Synthesis and FPGA implementation of Finite State Machines
9	Data path Modeling and Synthesis (Subsystem to be Defined by the Student)
10	Controller Modeling and Synthesis (Subsystem to be Defined by the Student)
11	Memory Subsystem Design
12	Power Aware Design of a simple subsystem
13	Case Study – RTL Architecture Modeling, Synthesis and FPGA Implementation of a Complete Digital System

Recommended Tools ModelSim,
Vivado

References

1. Michael D. Ciletti, *Advanced Digital Design with Verilog HDL*, Second Edition, Pearson Higher Education, 2011.
2. Morris Mano and Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, Fifth Edition, Pearson Higher Education, 2013.
3. Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, Third Edition, McGraw Hill, 2014.
4. Peter Minns and Lan Elliott, *FSMBased Digital Design Using Verilog HDL*, Fifth Edition, John Wiley and Sons Ltd, 2008.
5. Parag K. Lala, *Principles of Modern Digital Design*, Second Edition, John Wiley and Sons Ltd., 2007.

Evaluation Pattern

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Based on Lab Experiments, and Term Work with Report.

Functional Verification with Hardware Description Languages

21VL614 **3-0-0-3**

Learning Objectives

LO1 To provide a practical approach for verification of VLSI circuits.
LO2 To introduce hardware design languages for functional verification.
LO3 To emphasize the need and use of reusable verification environments.

Course Outcomes

CO1 Ability to understand the process of functional verification and its different methodologies.
CO2 Ability to apply methodologies to design a verification environment using System Verilog.
CO3 Ability to analyze the device under test and to write and simulate test-benches using System Verilog.
CO4 Ability to evaluate the verification process by use of assertion-based techniques.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	2	2
CO 3	-	-	3	2	-
CO4	-	-	3	-	-

Skills Acquired: Provide a practical approach for verification of designs using industry standard tools including System Verilog.

Course Contents

Unit 1: (15 hours)

HDL Review - Need for Functional Verification - ASIC Verification Concepts - Verification Tasks - Verification Plan - Linear Test Bench - Linear Random Test Bench - Self Checking Test Benches - Test Coverage - System Verilog for Design - Data types and Literals - Procedures and Procedural Statements - Operators - User-Defined Data Types - Hierarchy and Connectivity.

Unit 2: (15 hours)

System Verilog for Verification - Tasks - Functions - Interfaces - Verification Blocks Transaction Level Modeling - System Verilog Classes - Random Stimulus - Class-Based Randomization - Functional Coverage - Queues - Dynamic Arrays - Inter-Process Synchronization - System Verilog Assertions (SVA) - Assertion-Based Verification (ABV) - Boolean Expressions - Single and Multiple Clock Definitions - Implication Operators - System functions - Nested Implications - Immediate Assertions - Concurrent Assertions - Boolean Assertions - Sequences - Sequence Composition.

Unit 3: (15 hours)

Building a Testbench with Threads and Inter Process Communication - Functional Coverage Strategies - Parameterized Cover Groups - Coverage Data Analysis - Coverage Statistics Measurement - Complete System Verilog Test Bench Design - FSM Modeling with System Verilog - Verification of a Four Port Router: A Case Study.

References

1. Chris Spear, *SystemVerilog for Verification: A Guide to Learning the TestBench Language Features*, Third Edition, Springer, 2012.
2. Sutherland, Stuart, Davidmann, Simon, Flake, Peter, *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*", Second Edition, Springer Science & Business Media, 2006.
3. Faisal Haque, Jonathan Michelson, Khizar Khan, *The Art of Verification with System Verilog Assertions*, First Edition, Verification Central, 2006.
4. S Halsoun and T Sasao, *Logic Synthesis and Verification*, Kluwer Academic publishers, 2002.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

21VL615 Digital VLSI Testing & Testability 3-0-0-3

Learning Objectives

LO1 To introduce the concept of VLSI testing and testability.
LO2 To impart knowledge on the development of ATPG algorithms.
LO3 To comprehend the design for testability and explore the BIST concept.

Course Outcomes

CO1 Ability to understand the concept of testing and testability in VLSI circuits.
CO2 Ability to apply test pattern generation algorithms.
CO3 Ability to analyze built-in-test concepts.
CO4 Ability to design for testability in scan-based architectures.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	2
CO 2	-	-	3	3	3
CO 3	-	-	3	2	3
CO4	-	-	3	3	3

Skills Acquired: Development of testing algorithms and testable scan architectures.

Course Contents

Unit 1: (15 hours)

Concepts of VLSI Circuit Testing - Fault Modeling - Fault Collapsing - True Value Simulation - Fault Simulation - SCOAP Testability Measures - Combinational Circuit Test Generation - Roth's D Algorithm - PODEM ATPG Algorithms.

Unit 2: (15 hours)

Sequential Circuit Test Generation – Simulation based ATPG - Test Set Compaction - NDetect ATPG - Design for Testability - Ad Hoc Techniques - Level-Sensitive Scan Design - Scan Architectures and Testing - Scan design Rules - LFSR based Testing.

Unit 3: (15 hours)

Testable Logic Circuit Design - Logic BIST Architectures - Test Pattern Generation – Output Response Analysis - Test Stimulus Compression - Test Response Compaction - Memory BIST – RAM fault models - RAM Test Generation - Boundary Scan Architecture.

References

1. Vishwani D. Agrawal and Michael L. Bushnell, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Kluwer Academic Publishers, 2000.
2. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan &Claypool Publishers, 2009.
3. L. T. Wang, Cheng Wen Wu and Xiaoqing Wen, *VLSI Test Principles and Architectures – Design for Testability*, First Edition, Morgan Kaufmann Publishers, 2006.
4. L-T Wang, C. E. Stroud, & N. A. Touba, Editors, *System-on-chip Test architectures Nanometer design for testability*, Morgan Kaufmann Publishers, imprint of Elsevier, 2008.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

21VL683 ASIC Design and FPGA Lab 0-0-4-2

Learning Objectives

LO1 To provide a background in using SPICE based simulator for MOS based circuits.
LO2 To introduce VLSI design flow practically.
LO3 To impart understanding of design, oriented towards synthesis.

Course Outcomes

CO1 Ability to characterize and understand the fundamentals of MOSFET device and circuits.
CO2 Ability to analyze VLSI design flow using EDA tools.
CO3 Ability to demonstrate a synthesized system in hardware using any design level entry.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	2	2	3	3
CO 2	2	2	-	3	-
CO 3	2	2	-	2	-

Skills Acquired: Provide a practical exposure for designing and synthesis of subsystems using EDA tools through different levels of entries.

Lab Course Contents

Ex.No	Experiment details
1	MOSFET device and CMOS inverter characterization
2	CMOS NAND/NOR characteristics
3	Active loaded amplifier designs
4	Two stage CMOS OP-Amps with and without compensation technique
5	Logic Synthesis of ALU
6	Static Timing Analysis of gate level netlist
7	Placement and Routing of a sub-system
8	Design a CS amplifier and obtain its layout diagram, perform RC extraction and post layout simulation.
9	Implement ALU using FPGA

10	Implement an Up Counter using FPGA
11	Floating-Point Design Using the Vivado HLS Tool
12	Implementation of direct digital synthesizer using system generator

Recommended Tools
Xilinx Vivado, Xilinx HLS, Synopsys/Cadence

References
1. Sanjay Churiwala, *Designing with Xilinx® FPGAs: Using Vivado*, Springer 2017.
2. Sklyarov, V., Skliarova, I., Barkalov, A., Titarenko, L., *Synthesis and Optimization of FPGA-Based Systems*, Springer 2014.
3. Coussy, Philippe, Morawiec, Adam (Eds.), *High-Level Synthesis from Algorithm to Digital Circuit*, Springer 2008.
4. *Software manuals of Cadence/Synopsys.*

Evaluation Pattern:

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Based on Lab Experiments, and Term Work with Report.

Functional Verification Lab

21VL684 **0-0-4-2**

Learning Objectives
LO1 To provide a practical approach for verification of VLSI circuits.
LO2 To introduce object oriented programming for verification.
LO3 To impart knowledge of System Verilog as a tool for functional verification.

Course Outcomes
CO1 Ability to understand the basics of System Verilog RTL design and verification features.
CO2 Ability to apply object oriented principles to develop verification environment in System Verilog.
CO3 Ability to analyze the use of constrained random stimuli and coverage features for verification of designs.
CO4 Ability to create a verification environment in System Verilog for verifying any given DUT.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	3	-
CO 2	-	-	3	3	2

CO 3	2	-	3	3	-
CO4	2	-	3	3	2

Skills Acquired: Provides a hands-on approach for designing a verification testbench meeting industry specifications.

Lab Course Contents

Ex.No.	Experiment details
1	To design basic DUTs in System Verilog including latch/flipflops.
2	To familiarize with various array and array methodologies in System Verilog
3	Introducing System Verilog interfaces for block level communication.
4	Basic object oriented programming and classes in System Verilog
5	Understanding advanced OOP including inheritance and polymorphism for deep copying in system Verilog.
6	Use of randomization constraints in System Verilog.
7	Introducing threads, mailboxes and semphores for OOP based verification.
8	Understanding the use of generators and drivers
9	Understanding the use of monitors and reference models.
10	Creating scoreboard and environment for verification
11	Designing a complete verification test bench using System Verilog.

Recommended Tools
Synopsys, Questa Sim, Model Sim

References

1. Chris Spear, *System Verilog for Verification: A Guide to Learning the TestBench Language Features*, Third Edition, Springer, 2012.
2. Sutherland, Stuart, Davidmann, Simon, Flake, Peter, *SystemVerilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling*", Second Edition, Springer Science & Business Media, 2006.
3. Faisal Haque, Jonathan Michelson, Khizar Khan, *The Art of Verification with System Verilog Assertions*, First Edition, Verification Central, 2006.
4. S Halsoun and T Sasao, *Logic Synthesis and verification*, Kluwer Academic publishers, 2002.

Evaluation Pattern

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Based on Lab Experiments, and Term Work with Report.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

21RM613 Research Methodology 2-0-0-2

Learning Objectives

LO1 To enable defining and formulating research approaches towards obtaining solutions to practical problems.

LO2 To facilitate development of scientific oral and written communication skills. LO3 To comprehend the concepts behind adhering to scientific ethics and values.

Course Objectives

CO1 Ability to understand some basic concepts of research and its methodologies.

CO2 Ability to define and apply appropriate parameters and research problems.

CO3 Ability to develop skills to draft a research paper.

CO4 Ability to analyze and comprehend the ethical practices in conducting research and dissemination of results in different forms.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	2	2	3	-	2
CO 2	2	2	2	-	2
CO 3	3	2	3	-	3
CO4	3	2	2	3	3

Skills Acquired: Ability to Design, analyze and conduct research and comprehend the results.

Course Contents

Meaning of Research - Types of Research - Research Process - Problem Definition - Objectives of Research - Research Questions - Research design - Approaches to Research - Quantitative vs Qualitative Approach - Understanding Theory - Building and Validating Theoretical Models - Exploratory vs. Confirmatory Research - Experimental vs Theoretical Research - Importance of Reasoning in Research.

Problem Formulation - Understanding Modeling & Simulation - Conducting Literature Review - Referencing - Information Sources - Information Retrieval - Role of libraries in Information Retrieval - Tools for identifying Literatures - Indexing and Abstracting Services - Citation Indexes.

Experimental Research - Cause Effect Relationship - Development of Hypothesis
Measurement – Systems Analysis - Error Propagation - Validity of Experiments - Statistical Design of Experiments - Field Experiments - Data/Variable Types & Classification - Data Collection - Numerical and Graphical Data Analysis - Sampling - Observation - Surveys - Inferential Statistics - Interpretation of Results.

Preparation of Dissertation and Research Papers - Tables and Illustrations - Guidelines for Writing Manuscript - Abstract - Introduction - Methodology - Results and Discussion Conclusion - References - Citation - Listing System of Document.

Intellectual Property Rights (IPR) - Patents - Copyrights - Trademarks - Industrial Design - Geographical Indication - Ethics of Research - Scientific Misconduct - Forms of Scientific Misconduct - Plagiarism - Unscientific Practices in Thesis Work - Ethics in Science.

References

1. Bordens, K. S. and Abbott, B. B., *Research Design and Methods – A Process Approach*, 8th Edition, McGraw-Hill, 2011.
2. C. R. Kothari, *Research Methodology – Methods and Techniques*, 2nd Edition, New Age International Publishers.
3. Davis, M., Davis K., and Dunagan M., S*cientific Papers and Presentations*, 3rd Edition, Elsevier Inc.
4. Michael P. Marder, *Research Methods for Science*, Cambridge University Press, 2011.
5. T. Ramappa, *Intellectual Property Rights Under WTO*, S. Chand, 2008.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, *Intellectual Property in New Technological Age*. Aspen Law & Business; 6th Edition July 2012.
7. Tony Greenfield and Sue Greener., *Research Methods for Postgraduates*, 3rd Edition, John Wiley & Sons, Ltd. 2016.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Open Lab / Live-In Lab

21LIV604 **0-0-4-2**

Learning Objectives

LO1 To enable the students to acquire independent research aptitude.
LO2 To provide a platform to utilize the existing facilities / tools to address socially relevant problems.
LO3 To facilitate the design and development of a proof of concept system.

Course Outcomes

CO1 Ability to understand the research needs to address practical problems.
CO2 Ability to define and apply relevant concepts to the research problem.

CO3 Ability to develop a proof of concept system.
CO4 Ability to evaluate and analyse the results for further improvement.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	2	-	3	-	3
CO 2	2	-	3	-	3
CO 3	2	3	3	3	-
CO4	2	3	3	3	-

Skills Acquired: Ability to understand the research needs and develop a meaningful proof of concept system.

Course Contents
Design and development of a proof-of-concept system for the chosen problem.

Evaluation Pattern

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Based on Lab Experiments, and Term Work with Report.

Dissertation-Phase I

21VL798 **0-0-20-10**

Learning Objectives
LO1 To impart knowledge of computational and electronic concepts in communication systems.
LO2 To provide a platform for innovations in communication systems.
LO3 To facilitate the identification of the state-of-the-art research challenges communication.

Course Outcomes
CO1 Ability to define a research problem.
CO2 Ability to apply mathematical concepts to the research problem.
CO3 Ability to design and conduct independent research in the domain of interest. CO4 Ability to evaluate and analyze the outcomes of the research.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	3	3	-	-
CO 2	3	3	3	3	3
CO 3	3	3	3	3	3

CO4	3	3	3	-	3

Skills Acquired: Gain skills to design and perform independent research and evaluate and analyze the outcomes of the research.

Course Contents

Problems and Concepts may be Defined Based on Extensive Literature Survey by Standard Research Articles - Significance of Proposed Problem and the State-of-the-Art to be Explored - Industry Relevant Tools may be used for Demonstrating the Results with Physical Meaning and Create Necessary Research Components - Publications in Reputed Journals and Conferences may be Considered for Authenticating the Results.

Evaluation Pattern

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Can be Periodical Reviews, Demonstrations and Reports.

Dissertation-Phase II

21VL799 **0-0-28-14**

Learning Objectives

LO1 To impart knowledge of computational and electronic concepts in communication systems.

LO2 To provide a platform for innovations in communication systems.

LO3 To facilitate the identification of the state-of-the-art research challenges communication.

Course Outcomes

CO1 Ability to define a research problem.

CO2 Ability to apply mathematical concepts to the research problem.

CO3 Ability to design and conduct independent research in the domain of interest. CO4 Ability to evaluate and analyze the outcomes of the research.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	3	3	-	-
CO 2	3	3	3	3	3
CO 3	3	3	3	3	3
CO4	3	3	3	-	3

Skills Acquired: Gain skills to design and perform independent research and evaluate and analyze the outcomes of the research.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Course Contents

Problems and Concepts may be Defined Based on Extensive Literature Survey by Standard Research Articles - Significance of Proposed Problem and the State-of-the-Art to be Explored - Industry Relevant Tools may be used for Demonstrating the Results with Physical Meaning and Create Necessary Research Components - Publications in Reputed Journals and Conferences may be Considered for Authenticating the Results.

Evaluation Pattern

Assessment	Internal	External
*Continuous Assessment (CA)	70	NA
End Semester	NA	30
Total	70	30

*CA – Can be Periodical Reviews, Demonstrations and Reports.

21VL701 Semiconductor Device Modelling

3-0-0-3

Learning Objectives

LO1 To review the basic MOSFET structures and characteristics.
LO2 To impart knowledge on MOS models in simulation.
LO3 To introduce FINFETs and other multi-gate transistors.
LO4 To provide practical knowledge on design tools for device modelling.

Course Outcomes

CO1 Ability to understand the MOSFET structure evolution, types and working principle and multigate transistors..
CO2 Ability to apply the knowledge to model devices using simulation.
CO3 Ability to analyze the device behavior and characteristics of MOS using simulation.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	3	3
CO 2	-	-	3	3	3
CO 3	-	-	3	2	3
CO4	-	-	-	-	-

Skills Acquired: Provide a practical approach for device modeling using simulation tools.

Course Contents

Unit 1: (15 hours)

Introduction to MOSFET - Output and Transfer Characteristics - MOS Capacitor - Long, Short Channel MOSFETS - Non Ideal Effects - MOSFET Scaling - Threshold Voltage - Small Signal Model - Large Signal Model - MOSFET Parasitic Capacitances.

Unit 2: (15 hours)

SPICE Models for Semiconductor Devices - MOSFET Level1, Level2 and Level 3 Models - BSIM Model - Model Parameters - Models for Semiconductor Contacts and Hetero Junctions - Charge Control Models - Second Order Effects - Velocity Saturation and Universal Models - FINFETs - SOI MOSFETS - Single Gate to Multi Gate Transformation - Multigate MOSFET Technology - Physics of Multigate MOS - Mobility in Multi-gate MOSFET.

Unit 3: (15 hours)

Radiation Effects in Single Gate and Multi-Gate FETs - Single Event Effects – Multi-Gate MOSFET Circuit Design - Double Gate MOSFET - Drain Current Model - Scale Length - Fabrication Requirements and Challenges - SoC Design - Technology Aspects – Digital and Analog Circuit Design using WINSPICE.

References

1. B.G Streetman and S.K Banerjee, *Solid State Electronic Devices,* Seventh Edition, Prentice Hall India, 2010.
2. D.A.Neamen, *Semiconductor Physics and Devices: Basic Principle,* Third Edition, McGraw –Hill International, 2003.
3. J. P. Collinge, *FinFETs and Other Multi-Gate Transistors,* Springer, 2008.
4. Y.Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices,* Second Edition, Cambridge University Press, 2009.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

21VL702 VLSI Fabrication 3-0-0-3

Learning Objectives

LO1 To introduce the various crystal growth methods.
LO2 To impart knowledge on the effects of technology scaling in device fabrication.
LO3 To learn the fabrication techniques of BJT and MOSFETs.
LO4 To investigate the effects of process parameters in device fabrication.

Course Outcomes

CO1 Ability to understand the process of crystal growth used in IC fabrication.
CO2 Ability to understand the need for device scaling and its impact on device characteristics.
CO3 Ability to understand the fabrication flow of BJTs and MOSFETs.
CO4 Ability to apply the different process models to investigate the effects of varying process parameters on device characteristics.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	3
CO 2	-	-	3	2	3
CO 3	-	-	2	2	2
CO4	-	-	3	3	3

Skills Acquired: Provide an in-depth knowledge on how an IC is fabricated.

Course Contents

Unit 1: (15 hours)

Brief Review on Semiconductor Technology - Scaling Trends and Methodologies - Challenges in Scaling - ITRS Road map - Si Structure and Properties - Crystalline Directions in Silicon (Lattice Planes, Electron Arrangement) - Crystal Growth – CZ – Float Zone growth - Bridgman Growth - CMP & Polishing of Si Ingot - Defects in Silicon - Dopant/Impurity Segregation - Refining - SIMOX Process - Gettering - Thermal Oxidation Process - Deal Groove Model - Linear and Parabolic Rate Coefficients - Oxide Characterization – Ellipsometry.

Unit 2: (15 hours)

Photolithography - Optical Lithography - Positive/ Negative Photoresists - Resist Contrast and Profile - Resolution Limits - Depth of Focus - Resolving Power - Raleigh Resolution Criteria - Next Gen Photolithography - Etching - Wet Chemical Etching - Dry Etching - Plasma Assisted Etching - RIE - Diffusion - Basic Diffusion process - Ion Implantation – Range - Implant Damage - Annealing - Implantation Related Process - Film Deposition PVD/CVD - MOCVD - Atomic Layer deposition.

Unit 3: (15 hours)

Epitaxial Growth Techniques - Structures and Defects in Epitaxial layers - Dielectric Deposition – Poly-Si Deposition - Metallization - Process Integration - CMOS Technology - Low K Dielectrics - Strained Si - SiGe - SOI Technology - Multiple Gate MOSFETs Recent Trends.

References

1. Peter Vanzant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, Sixth Edition, McGraw Hill Professional, 2014.
2. Gary. S. May, S. M. Sze, *Fundamentals of semiconductor fabrication*, First Edition, John Wiley, 2003
3. Stephen A Campbell, *The Science and Engineering of Microelectronic Fabrication*, Second Edition, Oxford University Press, 2001.
4. James D. Plummer, Michael D. Deal, Peter B. Griffin, *Silicon VLSI Technology*: *Fundamentals, Practice and Modeling*, Prentice Hall India Private Limited, 2009.
5. S.Wolf , R.N.Tauber , S*ilicon Processing for the VLSI Era*, Lattice Press, 2000.
6. S.K.Ghandhi, *VLSI Fabrication Principles: Silicon and Gallium Arsenide*, Second Edition, Wiley India,2008.

Evaluation Pattern

Assessment	Internal	External

Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

VLSI Data Conversion Circuits

21VL703 **3-0-0-3**

Learning Objectives

LO1 To introduce basic concepts for understanding the design of data conversion circuits.
LO2 To introduce the design of basic ADCs (flash, SAR, Pipelined ADC).
LO3 To provide a practical approach of designing ADCs using circuit simulators.

Course Outcomes

CO1 Ability to understand the concepts of Nyquist and over-sampling ADCs.
CO2 Ability to apply concepts of SNDR and SFDR to model ADCs.
CO3 Ability to analyze non-linearity and mismatches in data conversion circuits.
CO4 Ability to evaluate data conversion circuits from top-level specifications and to model circuits using Verilog-A.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	-
CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired: To develop skills in designing industry standard ADC and DAC.

Course Contents

Unit 1: (15 hours)

ADC Terminologies - Static and Dynamic Characteristics - Flash ADC - Review of Basic Comparator Architectures – Kickback Noises - Switched Capacitor Circuits - Sample and Hold - Multiplying DAC - Flip Around and Non-Flip Around DACs - Gain and Bandwidth Requirements (Open and Closed Loop) - Spectral Properties of Sampled Signals - OverSampling and Anti-Aliasing Filters - FFT Logic and Rectangular Window - Bottom-Plate Sampling and Bootstrapped Switching - Charge Injection - Clock Feed Through - Charge Leakage - Verilog-A modeling for Comparators - Flash ADC - Sample and Hold circuit.

Unit 2: (15 hours)

Pipelined ADC - Basic DAC Architectures - R-2R - Binary-Weighted - Current-Steering DACs - SAR ADC - Power Delay Product and Figure-of-Merit Comparisons - Verilog-A modelling for SAR and Pipelined ADCs.

Unit 3: (15 hours)

Oversampling with Noise-Shaping Properties - Signal and Noise Transfer-Functions - First and Second Order Sigma-Delta Converters - Stability - Continuous-Time Delta-Sigma Converters - Inherent Noise Shaping Characteristics - Significance of Time-Domain ADCs - VCO-based ADC - Verilog-A modeling for Delta-sigma ADC and VCO based ADCs.

References

1. Razavi, B. *Principles of Data Conversion System Design*. IEEE Press, 1995.
2. Franco Maloberti, *Data Converters*, Springer Publishing company Inc., 2010.
3. Schreir, Richard and Gabor C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press, 2005.
4. Ximpeng Xing, Peng Zhu, Georges Gielen, *Design of Power-Efficient Highly Digital Analog-to-Digital Converters for Next Generation Wireless Communication Systems*, Springer International Publishing, 2018.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Semiconductor Memory Design

21VL704 **3-0-0-3**

Learning Objectives

LO1 To provide a basic understanding of the memory hierarchy and array structures in a system.

LO2 To introduce various semiconductor architecture and provide a platform to understand their limitations methodologies for improvement.

LO3 To provide a practical approach to memory design using cadence and Synopsys.

Course Outcomes

CO1 Ability to understand the various semiconductor memory architectures.

CO2 Ability to apply latch basics for designing SRAM and DRAM.

CO3 Ability to analyze fault modelling, reliability issues, radiation effects in memory design.

CO4 Ability to evaluate memory design aspects practically using design tools.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	-
CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired:
To gain experience in designing memories used in day-to-day technologies.

Course Contents

Unit 1: (15 hours)

Random Access Memory Technologies - SRAM Cell Structures - MOS SRAM Architecture - MOS SRAM Cell and Circuit Operation - Advanced SRAM Architectures and Technologies - Application Specific SRAMs - CMOS - DRAM - DRAM Cell Theory - Cell Structures - Soft Error Failure in DRAM.

Unit 2: (15 hours)

EEPROM Technology - Architecture - Non-volatile SRAM - Flash Memories - Advanced Flash Memory Architecture - RAM Fault Modeling - Volatile and Non-volatile Memory Testing Methods - RAM Fault Modeling - BIST Techniques for Memory - General Reliability Issues - RAM Failure Modes and Mechanism - Non-volatile Memory Reliability - Reliability Modeling and Failure Rate Prediction - Design for Reliability – Reliability Test Structures – Radiation Effects - Single Event Phenomenon (SEP) - FRAMs - GaAs - MRAMs - MCMs (2D and 3D).

Unit 3: (15 hours)

Advanced SRAMs - Leakage and Reliability - CAMs- Binary and Ternary CAMS - Embedded DRAMs - Resistive RAM and Circuits - Crossbar Arrays - 3D Flash - Process Technology and Circuits - Compute in Memory - Compute Near Memory - Neuromorphic Computing - Very High Density Memory Packaging - Schematic and Layout Issues for CMOS SRAM and DRAMS.

References

1. Ashok K. Sharma, *Semiconductor Memories: Technology, Testing, and Reliability*, Wiley, 2013.
2. Kevin Zhang,*Embedded Memories for Nano- Scale VLSIs*, Springer, 2009.
3. Santosh K. Kurinec and Krzysztof Iniewski, *Nanoscale Semiconductor Memories: Technology and Applications*, CRC press, 2013.
4. Koichi Ishibashi and Kenichi Osada, *Low Power and Reliable SRAM Memory Cell and Array Design*, Springer, 2011.
5. Haldun Hadimioglu, David Kaeli, Jeffrey Kuskin, Ashwin Nandam, JosepTorrellas, *High Performance Memory Systems*, Springer; 2004.
6. Saraju P. Mohanty and Ashok Srivastava, *Nano-CMOS and Post-CMOS Electronics: Circuits and Design*, Vol 2. (IET) The institution of Engineering and Technology, 2015.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Mixed Signal VLSI Design

21VL705 **3-0-0-3**

Learning Objectives

LO1 To introduce the concepts of mixed signal VLSI circuits.

LO2 To enhance design thinking capability by inculcating the importance of parameters like non-linearity, mismatches, noise and jitter in mixed signal circuit design.

LO3 To enrich the skills of computations by introducing modern engineering tools necessary for evaluating mixed signal circuits.

Course Outcomes

CO1 Ability to understand the working of various mixed signal circuits.

CO2 Ability to apply amplifier basics to design integrators, filters and switched capacitor circuits.

CO3 Ability to analyze non-linearity, mismatches, noise and jitters in mixed signal circuits.

CO4 Ability to evaluate mixed signal designs from top-level specifications and to model circuits using Verilog-AMS.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	-
CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired: To become skilled in designing the basic building blocks of mixed signal logic functions using high level descriptive languages.

Course Contents

Unit 1: (15 hours)

Sampling Theory - Spectral Properties of Sampled Signals - Oversampling -. Time Interleaved Sampling - Ping-Pong Sampling System - Analysis of Offset and Gain Errors Discrete Time Signals - Sample and Hold Circuits - Top and Bottom Plate Sampling- Characterizing Sample and Hold - Choice of Input Frequency - Anti-Alias Filter Design

Integrator-Based Filter - The gm-C Filter - Discrete Time Integrators - Filtering Topologies - The Bilinear Transfer Function - The Biquadratic Transfer Function - Filters Using Noise Shaping - Verilog-A Modeling of Filters.

Unit 2: (15 hours)

Switched Capacitor Circuits - Capacitors-Switches - Non-Overlapping Clocks - Resistor Equivalence - Parasitic Sensitive Integrator - Parasitic - Insensitive Integrators - SignalFlow-Graph Analysis - Parasitic Insensitive Switched Capacitor Amplifiers - Non Idealities - Finite Gain - DC Offset - Gain Bandwidth Product - Fully Differential Switched Capacitor Circuits - Noise in Switched-Capacitor Circuit - Verilog-A Modeling of Switched Capacitor Circuits.

Unit 3: (15 hours)

Basic Phase-Locked Loop Architecture - Voltage Controlled Oscillator - Analog Phase Detector - Digital Phase Detector - Loop Filer - PLL Design Example - Jitter And Phase Noise - Period Jitter - P-Cycle Jitter - Adjacent Period Jitter - Other Spectral Representations of Jitter - Probability Density Function of Jitter - Ring Oscillators - RC Phase Shift - LC Oscillators - Negative gm Oscillators - Verilog-A Modeling of VCO - Phase Detectors - Charge-pump - Loop Filters – PLL.

References

1. R. Jacob Baker, *CMOS Mixed Signal Circuit Design*, Wiley India Pvt. Ltd, 2008.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill, 2002, Reprint 2015.
3. R.Gregorian and G.C.Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley and Sons, 2004.
4. David A. Johns and Ken Martin, *Analog Integrated Circuit Design*, Wiley India Pvt. Ltd, 2008.
5. Kenneth S. Kundart and Olaf Zinke, *The Designer's Guide to Verilog- AMS*, Springer, 2004.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

CMOS RF IC Design

21VL706 **3-0-0-3**

Learning Objectives

LO1 To provide an overview of RF CMOS device characterization.

LO2 To enhance design thinking capability by bringing the importance of two port network parameters like MSG, MAG, Noise Figure, Stability, Linearity, Mismatches and Reflection Coefficients in RF IC designs.

LO3 To enrich the skills of computations by introducing modern engineering tools necessary for evaluating RF circuits.

Course Outcomes

CO1 Ability to understand RF CMOS device characteristics and its importance in RF ICs.

CO2 Ability to apply RF computational techniques to design actively loaded RF amplifiers.

CO3 Ability to analyze two port network parameters like Forward Gain, Noise Figure, Stability, Linearity, Mismatches and Reflection Coefficients in CMOS based RF sub blocks.

CO4 Ability to evaluate characteristics of RF CMOS sub blocks from top-level specifications and to model circuits using circuit simulators.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	-
CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired: Provides a platform to design RF CMOS amplifiers with the help of industry standard tools.

Course Contents

Unit 1: (15 hours)

Parallel RLC - Series RLC - Impedance Transformers - L-Pi-T-Type - Higher Order Matching - Transmission Lines - Driving Point Impedance - Artificial Lines - Microstrip -CPW - Small Signal RF CMOS Model - Noise Sources - Models - Distributed Gate Effects - Multi-Fingered Gate - Maximum Available Power Gain - Unity Power Gain Frequency.

Unit 2: (15 hours)

Two Port Network - S-Parameters - Maximum Stable Gain - Reflection Coefficients - Stability - Non-Linearity - 1-dB Gain Compression Point - Inter-Modulation - IIP3/OIP3 – Dynamic Range - RF Transmitter - Bit Error Rate - Signal to Noise Ratio - Sensitivity - Receiver Architecture - Direct Conversion - Super Heterodyne - Hartley Architecture - CMOS sub blocks - Low Noise Amplifier - Inductive Source Degeneration - Cascode and Differential Configurations - Inductive Peaking - Current Reuse.

Unit 3: (15 hours)

High Frequency Amplifier Design - Bandwidth Enhancement - Tuned Amplifiers - Broadband Monolithic Distributed Amplifier - Mixer Fundamentals - Nonlinear Systems as Linear Mixers - Active Down-Conversion Mixers - Single-Balanced - Double Balanced Gilbert Cell

Mixer - Class E - Stacked FET - Power Amplifiers for 60/77 GHz Bands - Doherty Power Amplifiers.

References

1. B. Razavi, *RF Microelectronics*, Second Edition, Pearson, 2012 (Indian Edition 2013 by Dorling Kindersley).
2. Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Second Edition, Cambridge University Press, 2004, Indian Reprint of 2009.
3. SorinVoinigescu, *High-Frequency Integrated Circuits*, Cambridge University Press, 2013, South Asian Paperback edition of 2018.
4. Michael Steer, *Microwave and RF Design - A Systems Approach*, SciTech Publishing, 2010, Indian Reprint by Yesdee Publishing, 2012.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

VLSI Signal Conditioning

21VL707 **3-0-0-3**

Learning Objectives

LO1 To introduce the concepts of operational transconductance amplifier (OTA) design.
LO2 To introduce the design of signal conditioning circuits using OTAs.
LO3 To provide a practical approach of evaluating signal condition circuits using circuit simulators.

Course Outcomes

CO1 Ability to understand the architecture of operational transconductance amplifiers (OTA).
CO2 Ability to apply Gm/Id techniques to design OTA and signal conditioning circuits.
CO3 Ability to analyze the effects of gain, bandwidth and timing mismatches in signal conditioning circuits.
CO4 Ability to evaluate signal conditioning circuits from top-level specifications and to model them using circuit simulators.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	-

CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired: Gain expertise in the design of industry standard signal conditioning circuits.

Course Contents

Unit 1: (15 hours)

Operational Trans-Conductance Amplifier basic Considerations - Application Requirements for OTAs used in Filters - The Case for Fully Differential Circuits - Transistor Models - g_m/I_D Based Design - Single-stage OTAs.

Unit 2: (15 hours)

Basic Differential Pair - Telescopic Architecture - Folded Cascode Architecture - Two-stage OTA - Gain Boosting - Common-Mode Feedback Implementation - Gm-C Biquad - TransConductor Implementation - NAUTA Cell - Source Follower Based Filter - Parameter Tuning - Q-tuning - VCF-tuning - Discrete Frequency Tuning / Programming - Tuning Gm over a Wide Range.

Unit 3: (15 hours)

Switched Capacitor Filters - First and Second Order Building Blocks - Sampled Data Operation - Bilinear Transformation - Cascade Filters - Switched Capacitor Integrators - Biquad Circuits - Switched Capacitor based PLL Design - Case Study of RF Receivers.

References

1. Schauman, Rolf and Van Valkenburg, *Design of Analog Filters*, Second Edition, Oxford University Press, 2009.
2. Tony Chan Carusone, David A. Johns and Kenneth W. Martin, *Analog Integrated Circuit Design*, Second Edition, John Wiley Inc., 2012.
3. 3. Gregorian and Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Optoelectronic Devices

21VL708 **3-0-0-3**

Learning Objectives

LO1 To provide an overview of working principles of opto-electronic devices.
LO2 To enable understanding the physics and performance parameters in optoelectronic devices.
LO3 To enable understanding of the working of critical optical components and integration schemes.
LO4 To impart knowledge on design and optimization of device performance.

Course Outcomes

CO1 Ability to understand fundamentals of optoelectronic devices such as photo detectors; LEDs and other such PN junction configurations.
CO2 Ability to apply concepts of device physics on the working principles of optoelectronic devices .
CO3 Ability to analyze optoelectronic device characteristics in detail using concepts from quantum mechanics and solid-state physics.
CO4 Ability to evaluate the device performance vis-à-vis suitable selection and optimization of electronic materials.

Skills Acquired: Design, integrate, analyze, and optimize the electronic characteristics of optoelectronic materials and devices.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	3
CO 2	-	-	3	2	3
CO 3	-	-	3	2	2
CO4	-	-	3	2	2

Course Contents

Unit 1: (15 hours)

Fundamentals of Elemental and Compound Semiconductors - An overview of Crystal Structures and Energy Bands - Electronic and Optical Processes in Semiconductors - Optoelectronic Materials - Semiconductors - compound semiconductors - III-V and II-VI Compounds - ZnO - ITO - GaN - GaA - Direct and Indirect Band Gap - Electronic Properties of Semiconductors - Fermi Level - Density of States - Life Time and Mobility of Carriers - Invariance of Fermi Level at Equilibrium - Diffusion - Continuity Equation - Excess Carriers - Quasi-Fermi Levels

Unit 2: (15 hours)

Optical Properties - Theory of Recombination - Radiative and Non-Radiative - Absorption Edge - Photoconductivity - Light Emitting Diodes - Device Configuration and Efficiency - LED Structures - Light Current Characteristics and Device Performance - Frequency Response and Modulation Band Width - Blue LED - Photodetectors - Performance Criteria of Photodetectors - Expressions for Quantum Efficiency - Responsivity - Photoconductors and Photodiodes - PIN Diodes - Heterojunction Diodes - Characteristics and Device Performance - High Speed Measurement Photoresistors - CCDs - Photomultiplier Tube - Noises in Photodetectors.

Unit 3: (15 hours)

Optical Systems and Fundamentals - Basics of Semi-conductor Optics - Confinement of Electron Waves - Optical Waveguides and Mode Theory - Semiconductor Optical Amplifiers (SOA) and Fabry-Perot Lasers - Coupled Mode Theory - DBR and DFB Lasers - Silicon Photonics - Integrated Optical Passive and Active Components - Tunable Filters - CMOS Technology - Electrical vs. Optical Interconnects - Overview of High-Speed Photonic Devices.

References

1. Ghatak A. and Thyagarajan K., *Optical Electronics*, Cambridge University Press, New Delhi, 1994.
2. Ben G. Streetmann & Sanjay Banerjee, *Solid State Electronic Devices*, Pearson 7th Edition, 2015.
3. Bhattacharya Pallab., *Semiconductor Optoelectronic Devices*, Pearson, 2nd Edition, 2017.
4. William S.C. Chang, *Fundamentals of guided wave optoelectronic Devices*, Cambridge University Press, 2009.
5. L. Pavesi, G. Guillot, *Optical interconnects: the silicon approach*, Springer, 2006.
6. C.F. Klingshirn, *Semiconductor Optics*, Springer, 2012.
7. Shun Lien Chuang, *Physics of Photonic devices*, John Wiley and Sons, 2009.
8. R. P. Khare, *Fiber Optics and Optoelectronics*, Oxford University Press, 2004

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA – Can be Quizzes, Assignments, and Term Work with Report.

Application Specific Integrated Circuits

21VL711 **3-0-0-3**

Learning Objectives

LO1 To introduce the design flow of different types of ASICs.
LO2 To import knowledge on partitioning, floor planning, placement, routing and logic synthesis.
LO3 To provide insight into System-on-Chip design and different types of communication architectures.

Course Outcomes

CO1 Ability to understand block level abstractions of ASIC design.
CO2 Ability to apply DRC on sub-section of ASICs.

CO3 Ability to analyze ASIC designs.
CO4 Ability to evaluate Platform and IP based SoC designs.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	2	-
CO 3	-	-	3	2	2
CO4	-	-	3	3	3

Skills Acquired: Design of Application Specific Integrated Circuits and performance analysis of SoCs.

Course Contents

Unit 1: (15 hours)

Introduction - Types of ASICs - Design Flow - Programmable ASICs – Antifuse - SRAM, EPROM - EEPROM based ASICs - Programmable ASIC Logic Cells and I/O Cells - Programmable Interconnects.

Unit 2: (15 hours)

ASIC Physical Design - System Partition - Partitioning - Partitioning Methods - Interconnect Delay Models and Measurement of Delay - Floor Planning - Placement - Routing - Global Routing - Detailed Routing - Special Routing - Circuit Extraction - DRC - Design Systems - Logic Synthesis - Half Gate ASIC - Schematic Entry - Low Level Design Language - PLA Tools -EDIF - CFI Design Representation.

Unit 3: (15 hours)

System-on-Chip Design - SoC Design Flow - Platform and IP based SoC Designs - Basic Concepts of Bus-Based Communication Architectures - On-Chip Communication Architecture Standards - Low-Power SoC Design.

References

1. J.S.Smith, *Application – Specific Integrated Circuits*, Pearson, 2003.
2. Dian Zhou, *Modern ASIC Design, Science Press*, China, 2011.
3. Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, *Low-Power NoC for High-Performance SoC Desig*, CRC Press, 2008.
4. S.Pasricha and N.Dutt, *On-Chip Communication Architectures System on Chip Interconnect*, Elsevier, 2008.
5. Gerardus Blokdyk, *Application-Specific Integrated Circuit ASIC A Complete Guide*, 5starcooks, 2018.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA

End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Low Power VLSI Circuit Design

21VL712 **3-0-0-3**

Learning Objectives

LO1 To provide a comprehensive idea about different sources of power dissipation in VLSI circuits.

LO2 To introduce the different power estimation and optimization methods. LO3 To apply low power techniques at all levels of the design cycle.

Course Outcomes

CO1 Ability to understand the concepts of low power VLSI circuits.
CO2 Ability to apply various architectures for low power implementations.
CO3 Ability to analyze the various power optimization techniques.
CO4 Ability to evaluate the power dissipation in VLSI circuits.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO1	-	-	2	-	3
CO2	-	-	2	2	2
CO3	-	-	3	2	2
CO4	-	-	2	2	2

Skills Acquired: Provide an understanding to analyze the different low power architectures.

Course Contents

Unit 1: (15 hours)

Importance of Low Power Consumption - Design for Low Power - Deep Submicron and Nanometer MOS Transistors and Models - Sources of Static and Dynamic Power Consumption in MOS Devices - New Device Technologies for Reducing Leakage Current - Basics of Power and Energy–Design and Test of Low Voltage CMOS – CMOS Inverters.

Unit 2: (15 hours)

Power Optimization During Design Cycle - Architecture - Algorithm and System Levels Power Optimization of Interconnects and Clocks - Dynamic Voltage Scaling - Clock Distribution - RTL Power Estimation and Optimization - Model Granularity - Model Parameters - Model Semantics - Model Storage and Model Construction.

Unit 3: (15 hours)

Power Optimization in Memories - Power in Cell Arrays - Power for Read and Write Accesses - Low Power Memory Technologies - Standby Power Optimization of Circuits and Systems - Power Optimization of Circuits and Systems During Operation - Low Power

Design Methodologies and Flows - Power Characterization and Modeling - Low Power Clock - Data and Power Gating - Adiabatic Switching Circuits - Battery-Aware Synthesis - CAD Tools for Low Power Synthesis - Case Study.

References

1. Jan M. Rabaey, *Low Power Design Essentials, Springer*, 2009.
2. Christian Piguet, *Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools*, CRC Press, Taylor and Francis, 2006.
3. Rakesh Chadha and J. Bhaskar, *An ASIC Low Power Primer, Analysis, Techniques and Specification*, Springer, 2013.
4. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, *Low power Methodology Manual for System on Chip*, Springer, 2007.
5. Kaushik Roy and S.C. Prasad, *Low power CMOS VLSI circuit design*, Wiley, 2000.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

FPGA based System Design

21VL713 **3-0-0-3**

Learning Objectives

LO1 To introduce the internal architecture of programmable logic with focus on FPGA.
LO2 To provide knowledge in FPGA design flow at the architectural and system design.
LO3 To impart a good background in block-based design using standard system level tools.

Course Outcomes

CO1 Ability to understand the structure of the fabric of programmable logic.
CO2 Ability to apply techniques for logic designing using field programmable devices.
CO3 Ability to analyze and comprehend FPGA design flow and related design, synthesis and timing issues.
CO4 Ability to evaluate system level architectures by integrating IP cores including softcore and hardcore processors.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	-
CO 3	-	-	3	2	-

CO4	-	-	3	2	2

Skills Acquired: Provide a practical approach for design of embedded systems using FPGAs.

Course Contents

Unit 1: (15 hours)

Programmable Logic Devices - PROM - PAL - PLA - CPLD - Gate Arrays - MPGA - FPGA - Programming Technologies - EPROM - EEPROM - FLASH - SRAM - FPGA Fabric - Configurable Logic Block - LUT - Slice - Slicem - Programmable Interconnects - Input Output Blocks - Keeper Circuit - Xilinx 7 Series Architecture.

Unit 2: (15 hours)

FPGA Design Flow and Abstraction Levels - Verilog Design for Synthesis - One Hot Encoding - Memory Blocks - Block Memory Generator (BRAM/BROM) - Single Port Memory - Dual Port Memory - FIFO - Distributed RAM - Synthesis Pitfalls - Latch Inference - Static Timing Analysis - Speed Performance - Timing Constraints - Clock Management - Clock Buffers - Clock Tree Routing.

Unit 3: (15 hours)

Introduction to SoC Design - Hard Macros - Multipliers - DSP Block - Hard Core Processors - Interface Circuits - Configuration Chain - JTAG Interface - Zynq7000 Architecture.

References

1. Amano, Hideharu, *Principles and Structures of FPGAs*, First Edition, Springer, 2018.
2. Readler, Blaine C., *Verilog by example: a concise introduction for FPGA design*, Full Arc Press, 2011.
3. ZainalabedinNavabi, *Embedded Core Design with FPGAs*, First Edition, McGraw Hill, 2008.
4. Xilinx Inc, *Vivado Design Suite User Guide*, 2021.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Electronic System Level Design

21VL714 **3-0-0-3**

Learning Objectives

LO1 To introduce design and verification at system level.

LO2 To introduce open-source language based design and debug.

LO3 To provide basics of Transaction Level Modelling and High-Level Synthesis. LO4 To introduce portable test and stimulus standards.

Course Outcomes

CO1 Ability to understand Electronic System level Design and Verification.
CO2 Ability to apply system level design methodologies using open-source languages.
CO3 Ability to analyze virtual prototyping and its advantages.
CO4 Ability to evaluate the transaction level models built using SystemC.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	2
CO 2	-	-	3	3	3
CO 3	-	-	3	3	2
CO4	-	-	3	3	3

Skills Acquired: System level modelling and verification.

Course Contents

Unit 1: (15 hours)

Introduction to Electronic System Level Design - Hybrid Design - ESLD Flows and Methodologies - Architecture Exploration - Hardware-Software Partitioning.

Unit 2: (15 hours)

Models for ESL Design - Open-Source Languages - Specc - Archc and Systemc - Transaction Level Modelling - Building Platform Models - High Level Synthesis - Power Evaluation - Virtual Platform and Virtual Prototyping.

Unit 3: (15 hours)

Functional Models - High Level Verification - Formal Solution - Debugging Platform Models Case Study - Bluespec and Accellera Initiatives on Test and Stimulus Standards - Property Specification Language.

References

1. Sandro Rigo, Rodolfo Azevedo and Luizsantos, *Electronic System Level Design – An Open Source Approach*, Springer, 2011.
2. Bailey, Brian, and Grant Martin. *ESL Models and their Application*, Springer, Boston, MA, Springer, USA, DOI 10 (2010): 978-1.
3. David Black, Jack Donovan, Bill Bunton and Anna Keist, *System C from the ground up*, Second Edition, Springer, 2010.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA

End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

System-on-Chip & FPGA Testing

21VL715 **3-0-0-3**

Learning Objectives

LO1 To introduce the modules of System-on-chip.
LO2 To impart knowledge on the FPGA Architecture.
LO3 To comprehend the testing process on architectures.

Course Outcomes

CO1 Ability to comprehend the concept of VLSI testing.
CO2 Ability to apply testing process on VLSI Architectures.
CO3 Ability to analyze the challenges in FPGA Testing.
CO4 Ability to design for testability and built-in test architectures.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	-	2
CO 2	-	-	3	3	3
CO 3	-	-	3	2	3
CO4	-	-	3	3	3

Skills Acquired: Knowledge on System on Chip Testing and FPGA Testing.

Course Contents

Unit 1: (15 hours)

Importance of System-On-Chip Testing - Boundary Scan - Core-Based Testing - SoC Design Examples - System-on-Chip (SoC) Testing - Modular Testing of SoCs - Test Scheduling - Modular Testing of Hierarchical SoCs.

Unit 2: (15 hours)

Field Programmable Gate Array Testing - FPGA Architecture - Configuration - Testing Approaches - BIST of Programmable Resources - Logic Resources - Interconnect Resources - Embedded Processor - Based Testing.

Unit 3: (15 hours)

Built-in-Self-Test - Low Power BIST - Vector Filtering BIST - Power - Aware Test Scheduling - Built-in Logic Block Observer - Self-Testing Using an MISR - LSSD On-Chip Self-Test - Design and Test Practice - Case Studies - SoC Testing for PNX8550 System Chip - Industry Application Notes.

References

1. L-T Wang, C. E. Stroud, & N. A. Touba, Editors, *System-on-chip Test architectures Nanometer design for testability,* Morgan Kaufmann Publishers, imprint of Elsevier, 2008.
2. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan & Claypool Publishers, 2009.
3. Cheng-Wen Wu, Chih-Tsun Huang, *Essential Issues in SOC Design*, Youn- Long Steve Lin, Editors, Soc Testing and Design for Testability pp 265-310, 2006.
4. https://www.electronicsforu.com/technology-trends/benefits-of-soc-incircuit-testing, 2020.
5. FPGA Automatic Test Equipment - Intel® FPGA https://www.intel.in/content/www/in/en/design/test-and-validate/programmable applications.html. 2021.
6. http://www.ee.ncu.edu.tw/~jfli/test1/lecture/ch09.
7. https://www.cs.ccu.edu.tw/~pahsiung/courses/soc/notes/05_Testing.pdf.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

VLSI Architectures for Multicore and Heterogeneous Computing

21VL721 **3-0-0-3**

Learning Objectives

LO1 To introduce approaches to parallelism in modern processors.
LO2 To impart background in communication and memory management schemes in multicore systems.
LO3 To provide grounding in the fundamentals of heterogeneous computing systems. LO4 To introduce typical paradigms in heterogeneous systems.

Course Outcomes

CO1 Ability to understand approaches to parallelism in processors.
CO2 Ability to apply parallel approaches to analyze computing systems.
CO3 Ability to analyze the impact of communication and memory architectures on performance.
CO4 Ability to evaluate the design requirements of applications to be implemented in computing platforms.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	-	-	2
CO 2	-	-	3	-	2

CO 3	-	-	3	-	2
CO4	-	-	3	-	2

Skills Acquired: Ability to analyze different computing approaches used in processors and evaluate impact of architecture, communication and memory on computing approaches to different problems.

Course Contents

Unit 1: (15 hours)

Review of Types of Parallelism - Instruction Level Parallelism - Thread Level Parallelism - Limits of ILP - Parallel Processing Architectures - Superscalar - VLIW - Scheduling - Techniques - Static and Dynamic Schemes - SIMD Architectures - GPU.

Unit 2: (15 hours)

Inter-Processor Communication Schemes - Bus-Based - Shared Memory - Distributed Memory and Network on Chips - Performance Analysis - Data Parallelism - GPU and GPGPU Applications - Overview of HPC Platforms - CUDA/Hadoop/Mapreduce.

Unit 3: (15 hours)

Introduction to Markovian/Stochastic Models for Heterogeneous Computing - Operating System - Role of Multi-Cores - Case Study for Heterogeneous Architectures - Case Studies of Data-Intensive Application Platforms - FPGA based Platforms.

References

1. Hennesey and Patterson, *Computer Architecture: A Quantitative Approach*, Fifth Edition, Morgan Kaufmann, 2012.
2. K. Uchiyama, F. Arakawa, H. Kasahara, T. Nojiri, H. Noda, Y. Tawara, A. Idehara, K. Iwata and H. Shikano, *Heterogeneous Multi-core Processor Technologies for Embedded Systems*, Springer, 2012.
3. J. Dongarra and A.L. Lastovetsky, *High Performance Heterogeneous Computing*, Wiley Series, 2009.
4. Abderazek Ben Abdallah, *Advanced Multicore Systems-On-Chip: Architecture, On-Chip Network, Design*, Springer 2017.
5. Journals, White papers and Technical Reports in the area of High-Performance Parallel computing.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design
Emerging Architectures for Machine Learning

21VL722 3-0-0-3

Learning Objectives

LO1 To introduce new paradigms in computing.
LO2 To familiarize various aspects and issues in implementation of machine learning systems.
LO3 To impart background on application of FPGAs and unconventional computing platforms for machine learning.
LO4 To provide exposure to using state of the art computing tools.

Course Outcomes

CO1 Ability to understand high performance machine learning architectures.
CO2 Ability to apply computing paradigms for machine intelligence problems.
CO3 Ability to suggest solutions and platforms for dataflow intensive problems.
CO4 Ability to evaluate the use of diverse technologies to design efficient applications.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	3	2
CO 2	-	-	3	3	2
CO 3	-	-	3	3	2
CO4	-	-	3	3	2

Skills Acquired: Ability to develop architectures for Machine Learning.

Course Contents

Unit 1: (15 hours)

Computing Platforms for Machine Learning - Processors - GPU and Gpgpus - FPGA Platforms - SBC Platforms - Cloud and Hadoop - Overview of IoT.

Unit 2: (15 hours)

Custom Architectures - Neural Network Architectures - Spike Neural Networks - Cellular Neural Network - Generational Adversarial Networks (Gans) - Quality Metrics and Implementation Issues.

Unit 3: (15 hours)

Case Studies in Digital Technologies and Cyber Physical Systems - Security for IoT and Cloud - Assurance of Integrity - Security and Confidentiality.

References

1. David B. Kirk, Wen-Mei W. Hwu, *Programming Massively Parallel Processors: A Hands-on Approach*, Second Edition, Morgan Kauffman, 2016.
2. Bertil Schmidt, *Bioinformatics: High Performance Parallel Computer Architectures*, CRC Press, 2011.
3. Journal Articles and White Papers.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Wavelets and Applications

21VL723 **3-0-0-3**

Learning Objectives

LO1 To understand the concepts of Continuous and Discrete Wavelet Transform.
LO2 To introduce Filter Bank design using wavelets.
LO3 To understand design of wavelets for various application fields.
LO4 To provide a practical approach for VLSI architecture design using wavelets.

Course Outcomes

CO1 Ability to understand the need for time frequency analysis.
CO2 Ability to apply methodologies to filter bank design for multiresolution analysis. CO3 Ability to apply wavelet design concepts for signal and image processing.
CO4 Ability to apply the concepts of wavelets to develop algorithms for VLSI architecture design.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	2	2	2
CO 2	-	-	2	2	2
CO 3	-	-	3	3	2
CO4	-	-	3	3	3

Skills Acquired: Provide a practical approach for design of VLSI architecture for signal and image processing.

Course Contents

Unit 1: (15 hours)

Review of Mathematical Preliminaries - Vector/Function Space - Basis Function - Inner Product - Orthogonality - Orthogonal Complement - Review of Fourier Theory and Properties of Fourier Transform - Short Time Fourier Transform - Heisenberg's Uncertainty Principle -Continuous Wavelet Transform (CWT) and Its Properties - Discrete Wavelet Transform (DWT) - Haar Scaling Function - Nested Spaces - Wavelet Function - Designing Orthogonal Wavelet Systems (Daubechies – Coiflet - Symlet Wavelet System Coefficients).

Unit 2: (15 hours)
Signal Decomposition using DWT - Relation to Filter Banks and Frequency Response - Signal Reconstruction using DWT - M Band Wavelets - Multi Resolution Analysis - Applying Methodologies to Filter Bank Design for Multiresolution Analysis - Design of Biorthogonal Wavelets - Lifting Scheme - Applying Methodologies to Filter Bank Design for Multiresolution Analysis - Wavelet Applications - Transform Coding - Channel Coding - Audio Compression - Image Compression - Denoising - Image Fusion - Object Isolation.

Unit 3: (15 hours)
Algorithm Views of Discrete Wavelet Transform - Practical Design Examples of 2-D DWT - JPEG 2000 Encoder Systems - Architectures of Motion - Compensated Temporal Filtering (MCTF) - Design of a Reconfigurable Architecture for Discrete and Continuous Wavelet Transforms - Design of Reusable Silicon IP Cores for Discrete Wavelet Transform Applications.

References

1. K. P. Soman, K. I. Ramachandran, *Insight into Wavelets : From Theory to Practice*, Third Edition, PHI, 2010.
2. Gilbert Strang, *Introduction to Linear Algebra*, Fourth Edition, Wellesley-Cambridge Press, Fifth Edition, 2016.
3. Liang-gee Chen, Chao-tsung Huang, Ching-yeh Chen, Chih-chi Cheng, *VLSI Design of Wavelet Transform: Analysis, Architecture, and Design Examples*, First Edition, Imperial college press, 2006.
4. Gilbert Strang, Truong.Nguyen, *Wavelets and Filter banks*, Wellesley Cambridge Press, Second Edition, 1996.
5. Sidney Burrus C, *An Introduction to Wavelets*, Academic press, 2014.
6. Stark, Hans-Georg, *Wavelets and signal processing: An application based introduction*, Springer, 2005.
7. P. P. Vaidyanathan, *Multirate Systems and Filter Banks*, Pearson Education, 2004.
8. Stephane G Mallat, *A Wavelet Tour of Signal Processing*, The sparse way Academic Press, Third edition, 2008.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Data Structures and Algorithms

21VL724 **3-0-0-3**

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design

Learning Objectives

LO1 To introduce the linear and non-linear data structures and explore its applications.
LO2 To provide representation using graph data structure.
LO3 To impart knowledge of basic sorting and searching algorithm.
LO4 To instill the concept of designing efficient algorithms using data structures.

Course Outcomes

CO1 Ability to understand linear and non-linear data structures.
CO2 Ability to apply appropriate data structures to solve computational problems.
CO3 Ability to analyze the algorithms and its complexity.
CO4 Ability to design and employ algorithms using relevant data structures in real-time applications.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	2
CO 2	-	-	3	-	3
CO 3	-	-	3	2	3
CO4	-	-	3	3	3

Skills Acquired: Design of algorithms and problem-solving using data structures.

Course Contents

Unit 1: (15 hours)

Algorithm Analysis - Methodologies for Analyzing Algorithms - Asymptotic Notation - Recurrence Relations - Data Structures - Linear Data Structures - Stacks - Queues – Linked - Lists - Vectors - Trees - Binary Search Trees - AVL Trees - Red-Black Trees - B-Trees - Hash-Tables - Dictionaries - Associative Arrays - Database Indexing - Caches - Sets.

Unit 2: (15 hours)

Searching and Sorting - Insertion and Selection Sort - Quick Sort - Merge Sort - Heap Sort - Bucket Sort and Radix Sort - Comparison of Sorting Algorithms and Lower Bounds on Sorting - Fundamental Techniques - The Greedy Method - Divide and Conquer.

Unit 3: (15 hours)

Dynamic Programming - Graph Algorithms - Breadth-First Search - Depth-First Search - Topological Sort - Strongly Connected Components - Minimum Spanning Trees – Single Source Shortest Paths - All-Pairs Shortest Paths - Maximum Flow - Network Flow and Matching - Flows and Cuts.

References

1. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest and Clifford Stein, *Introduction to Algorithms*, Third Edition, MIT Press, 2009.
2. Robert Sedgewick and Kevin Wayne, *Algorithms*, Fourth Edition, Addison Wesley, 2011.
3. Kurt Mehlhorn and Peter Sanders, *Data Structures and Algorithms: The Basic Toolbox,* Springer, 2008.

4. John V. Guttag, *Introduction to Computation and Programming using Python*, MIT Press, second edition, 2016.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Reconfigurable Computing

21VL725 **3-0-0-3**

Learning Objectives

LO1 To introduce the methodology of reconfigurable computation.
LO2 To provide a background on reconfiguration requirement and management.
LO3 To impart experience in designing and mapping reconfigurable systems.
LO4 To orient applications catering power, area and performance requirements.

Course Outcomes

CO1 Ability to understand reconfigurable architectures.
CO2 Ability to introduce architecture that enables high performance computation as well as the supporting application mapping process.
CO3 Ability to analyze different opportunities for the use of reconfigurable architectures.
CO4 Ability to evaluate the requirements of reconfigurable hardware.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	2	2	-
CO 3	-	-	2	3	2
CO4	-	-	2	3	2

Skills Acquired: Provides a detailed insight about various reconfigurable architectures and its requirements.

Course Contents

Unit 1: (15 hours)

Reconfigurable Logic Devices - Reconfigurable Computing Hardware - Survey of FPGA and Non-FPGA Devices - Fine Grained – Coarse Grained - Reconfiguration Management - Partial Reconfiguration and Hierarchical Design.

Unit 2: (15 hours)
Programming Reconfigurable Systems - Languages and Compilation - Reconfigurable Computing Systems - Mapping Applications to Reconfigurable Systems.

Unit 3: (15 hours)
High-Level Synthesis - Area-Performance - Power-Aware Mapping - Placement - Layout and Routing - Application Development - Case Study with Applications and Solutions from Different Domains.

References

1. Scott Hauck and Andre *Dehon, Reconfigurable Computing: The Theory and Practice of FPGA Based Computation*, Elsevier,2008.
2. Gokhale, Maya B., Graham, Paul S., *Reconfigurable Computing - Accelerating Computation with Field-Programmable Gate Arrays*, Springer 2007.
3. Christophe Bobda, *Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications*, Springer 2007.
4. Churiwala, Sanjay (Ed.), *Designing with Xilinx® FPGAs Using Vivado*, Springer 2017.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

VLSI Signal Processing

21VL726 **3-0-0-3**

Learning Objectives

LO1 To introduce the concepts of DSP architecture design.
LO2 To provide an understanding of the techniques needed for the implementation of DSP architectures.
LO3 To emphasize the realization of DSP architectures with high throughput, less area and less power.
LO4 To provide an understanding of the concepts of high-performance VLSI system design.

Course Outcomes

CO1 Ability to understand the various VLSI architectures for digital signal processing algorithms.
CO2 Ability to apply and analyze techniques of high-level architectural transformation for designing DSP algorithms.

CO3 Ability to apply and analyze the algorithmic transformation techniques for designing DSP algorithms.
CO4 Ability to evaluate architectures for adders, multipliers and digital filters.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	2	-
CO 3	-	-	3	2	-
CO4	-	-	3	3	3

Skills Acquired: Provides skill needed for the design and implementation of VLSI architectures for DSP algorithms.

Course Contents

Unit 1: (15 hours)
Introduction to Digital Signal Processing Systems - Iteration Bound - Pipelining and Parallel Processing - Retiming- Unfolding - Folding - Systolic Architecture Design.

Unit 2: (15 hours)
Fast Convolution - Algorithmic Strength Reduction - Pipelined and Parallel Recursive and Adaptive Filters - Scaling and Round Off Noise - Digital Lattice Filter Structures.

Unit 3: (15 hours)
Bit-Level Arithmetic Architectures - Redundant Arithmetic - Numeric Strength Reduction - Low-Power Design - Case Study High-Level Algorithm and Architecture Transformations for DSP Synthesis.

References

1. Keshab K. Parhi, *VLSI Digital Signal Processing Systems, Design and Implementation*, Wiley, Indian Reprint, 2007.
2. U. Meyer – Baese, *Digital Signal Processing with Field Programmable Arrays*, Springer, Second Edition, Indian Reprint, 2007.
3. S.Y.Kuang, H.J. White house, T. Kailath, *VLSI and Modern Signal Processing*, Prentice Hall, 1995.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Department of Electronics and Communication Engineering
Curriculum 2021
M.Tech VLSI Design
Static Timing Analysis

21VL727 **3-0-0-3**

Learning Objectives

LO1 To introduce timing analysis and apply it to constrain a design.
LO2 To impart knowledge on cell delay calculation and parasitic extraction.
LO3 To provide a practical approach for configuring static timing environment. LO4
To analyze a timing report and check for timing violations.

Course Outcomes

CO1 Ability to understand the process of timing analysis in circuits and system design.
CO2 Ability to apply wire load models to compute the cell delay.
CO3 Ability to analyze the circuit for design violations by configuring. CO4
Ability to evaluate the system and perform timing verification.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	2	3
CO 2	-	-	3	3	2
CO 3	-	-	3	3	3
CO4	-	-	3	3	3

Skills Acquired: Provide a practical approach for timing analysis of designs using standard tools like Synopsys PrimeTime.

Course Contents

Unit 1: (15 hours)

Introduction to STA - Concepts - Standard Cell Library - Pin Capacitance - Timing Modeling - Timing Models for Combinational and Sequential Cells - State Dependent Models - Advanced Timing Modeling - Power Dissipation Modeling - Other Attributes in Cell Library - Characterization and Operating Conditions - Interconnect Parasitics.

Unit 2: (15 hours)

Delay Calculation - Overview - Cell Delay using Effective Capacitance - Interconnect Delay - Slew Merging - Different Slew Thresholds - Different Voltage Domains - Path Delay and Slack Calculation - Crosstalk and Noise - Glitch Analysis - Delay Analysis - Computational Complexity - Noise Avoidance Techniques - Configuring the STA Environment.

Unit 3: (15 hours)

Specifying Clocks - Generated Clocks - Constraining Input - Output Paths - Timing Path Groups - Modeling of External Attributes - Design Rule Checks - Virtual Clocks - Refining the Timing Analysis - Point to Point Specification - Path Segmentation - Timing Verification - Setup - Hold Timing Check - Multicycle - False - Half Cycle Paths - Removal and Recovery Timing Checks - Timing Across Clock Domains - Multiple Clocks - Interface Analysis - Statistical Static Timing Analysis.

References

1. J. Bhasker, R.Chadha, *Static Timing Analysis for Nanometer Designs: A Practical Approach*, Springer, 2009.
2. Charles J. Alpert Dinesh P. Mehta Sachin S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, First edition,CRC Press, 2009.
3. Himanshu Bhatnagar, *Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time*, Second Edition, Kluwer Academic Publishers, 2002.
4. Sridhar Gangadharan , Sanjay Churiwala, *Constraining Designs for Synthesis and Timing Analysis:A practical Guide to Synopsys Design Constraints*, Springer,2013.
5. R.Jayagovwri, Pushpendra S Yadav , *Static Timing Analysis for VLSI Circuits*, First Edition, Medtech, Scientific International Publisher,2018.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Computer Aided Design for VLSI Circuits

21VL728 **3-0-0-3**

Learning Objectives

LO1 To introduce physical design cycle.
LO2 To introduce VLSI Design methodologies and provide an understanding of the VLSI design automation tools.
LO3 To emphasize placement, floor planning and routing and synthesis.

Course Outcomes

CO1 Ability to understand the VLSI physical design cycle.
CO2 Ability to apply the VLSI design automation tools.
CO3 Ability to analyze placement, floor planning and routing algorithms. CO4 Ability to evaluate combinational logic synthesis.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	2	-
CO 3	-	-	3	3	3
CO4	-	-	3	3	3

Skills Acquired: Provide a platform for understanding and applying CAD tools for VLSI physical design.

Course Contents

Unit 1: (15 hours)

VLSI Design Methodologies - Basics of VLSI Design Automation Tools - Data Structures for the Representation of Graphs - Computational Complexity - Combinatorial Optimization Problems - Decision Problems - Complexity Classes.

Unit 2: (15 hours)

VLSI Physical Design Cycle - Placement Algorithms – Partitioning – Kernighan-Lin Partitioning Algorithm - Terminology and Floor Plan Representation-Optimization Problems in Floor Planning - Types of Local Routing Problems - Classification of Compaction Algorithms.

Unit 3: (15 hours)

Combinational Logic Synthesis - Binary Decision Diagrams - Hardware Models for High Level Synthesis - Allocation - Assignment and Scheduling - Scheduling Algorithms.

References

1. S.H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2002.
2. N.A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, *VLSI Physical Design automation: Theory and Practice*, World Scientific 1999.
4. K. Golshan, *Physical Design Essentials: An ASIC Design Implementation Perspective*, Springer, 2010.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Cryptography

21VL731 **3-0-0-3**

Learning Objectives

LO1 To provide basic knowledge and skills in the fundamental theories and practices of data security.

LO2 To provide an overview of the field of security and assurance emphasizing the need to protect information being transmitted electronically.
LO3 To realize the hardware architectures of cryptographic algorithms.

Course Outcomes

CO1 Ability to understand the mathematical fundamental concepts needed for cryptographic algorithm implementations.
CO2 Ability to apply concepts of security to computing systems.
CO3 Ability to analyze cryptosystems architecture, digital signature algorithms and secure data sharing techniques.
CO4 Ability to evaluate the implementation of cryptographic algorithms in FPGA.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	2	-
CO 3	-	-	3	2	-
CO4	-	-	3	3	3

Skills Acquired: Application to implement cryptographic algorithms.

Course Contents

Unit 1: (15 hours)

Introduction to Probability Theory - Information Theory - Complexity Theory and Number Theory - Private-Key - Cryptosystems - Classical Ciphers - DES Family - Product Ciphers - Lucifer Algorithm - Modern Private Key Cryptographic Algorithms - Differential Cryptanalysis - Linear Cryptanalysis - S-Box Theory - Propagation and Nonlinearity - Construction of Balanced Functions.

Unit 2: (15 hours)

Public-Key Cryptosystems - RSA Cryptosystem - Merkle-Hellman Cryptosystem - Mceliece Cryptosystem - Elgamal Cryptosystem - Elliptic Curve Cryptosystems - Probabilistic Encryption - Pseudo-Randomness - Polynomial Indistinguishability - Pseudorandom Bit Generators - Pseudorandom Function Generators - Super Pseudorandom Permutation Generators - Hashing - Theoretic Constructions - Hashing Based on Cryptosystems - MD Family - SHA Family - Keyed Hashing.

Unit 3: (15 hours)

Digital Signature - Generic Signature Schemes - RSA Signatures - Elgamal Signatures - Blind Signatures - Undeniable Signatures - Fail-Stop Signatures - Time Stamping - Secret Sharing - Threshold Secret Sharing (T, T) - Threshold Schemes - Shamir Scheme - Blakley Scheme - Modular Scheme - General Secret Sharing - Stream Ciphers - Linear Complexity - Non-Linear Feedback Shift Registers - VLSI Implementation of Some of the Cryptographic Algorithms.

References

1. Josef Pieprzyk, Thomas Hardjono and Jennifer Seberry, *Fundamentals of Computer Security,* Springer, 2003.

2. Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, *Handbook of Applied Cryptography*, CRC Press, 1996.
3. Abhijith Das and VeniMadhavanC. E., *Public-key Cryptography, Theory and Practice,* Pearson Education, 2009.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Network on Chip

21VL732 **3-0-0-3**

Learning Objectives

LO1 To provide basic concepts of NoC design by introducing the topologies, router design and MPSoC styles.
LO2 To introduce sample routing architectures with evaluation and routing algorithm on a NoC.
LO3 To provide knowledge of the functions of reconfiguarable NoC. LO3
To introduce 3D NoCs and its future trends.

Course Outcomes

CO1 Ability to understand the need for NoC, architectures, reconfiguration NoCs.
CO2 Ability to understand routing algorithms and flow control mechanisms.
CO3 Ability to analyze and design aspects of NoC architecures and reconfiguration techniques.
CO4 Ability to analyze and design aspects of NoC routing algorithms and flow control mechanisms.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO1	-	-	2	-	-
CO2	-	-	2	-	-
CO3	-	-	3	3	2
CO4	-	-	3	3	2

Skills Acquired: To become skilled in the design aspects of NoC topologies, routing algorithms and reconfigurable NoCs.

Course Contents

Unit 1: (15 hours)
Topology Design - Introduction - On-Chip Vs. Off-Chip Networks - On-Chip Network Building Blocks. Interface with System Architecture - Shared Memory Networks in Chip Multiprocessors - Synthesized Nocs in Mpsocs. Topology - Direct Topologies - Indirect Topologies - Irregular Topologies. Routing Algorithms - Types - Oblivious Routing - Adaptive Routing - Source Routing - Node Table-Based Routing - Routing on Irregular Topologies.

Unit 2: (15 hours)
Flow Control - Message-based Flow Control - Packet-based Flow Control - Flit-based Flow Control - Flow Control Implementation in MPSoCs - Router Microarchitecture - Pipeline - Buffer Organization - Allocators and Arbiters - Architecture Design of Network-On-Chip - Wormhole Router Architecture Design - Adaptive Router Architecture Design.

Unit 3: (15 hours)
Evaluation of Network-On-Chip Architectures - Traffic Modeling - Localized Traffic - Reconfigurable Network-On-Chip Design - Local Reconfiguration Approach - Topology Reconfiguration - Link Reconfiguration - Three-Dimensional Integration of Network-OnChip - Opportunities and Challenges of 3D Integration - Design and Evaluation of 3D NoC Architecture - Future Trends - Photonic NoC - Wireless NoC.

References

1. Santanu Kundu, Santanu Chattopadhyay, *Network-on-Chip: The Next Generation of System-on-Chip Integration*, CRC Press, 2018.
2. N. Enright Jerger and L-S. Peh, *On-Chip Networks, Synthesis Lectures on Computer Architecture*, Morgan & Claypool, 2009.
3. Konstantinos Tatas, Kostas Siozios, Dimitrios Soudris, Axel Jantsch, *Designing 2D and 3D Network on Chip Architecture*, Springer, 2013.
4. A Jantsch and H. Tenhunen, *Networks on Chip*, Kluwer Academic Publishers, 2003.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Hardware Software Co-Design

21VL733 **3-0-0-3**

Learning Objectives
LO1 To introduce the design of mixed hardware-software systems.
LO2 To partition simple software programs into hardware and software components.

LO3 To identify performance bottlenecks in a given hardware-software architecture.
LO4 To introduce optimization approaches to transformations on hardware and software components.

Course Outcomes

CO1 Ability to understand the need for hardware software codesign in the design flow process.
CO2 Ability to analyze hardware-software co-design problems for systems with moderate Complexity.
CO3 Ability to apply hardware-software co-design methods and techniques to practical problems.
CO4 Ability to apply different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	3	-
CO 2	-	-	3	3	-
CO 3	-	-	3	3	3
CO4	-	-	3	3	3

Skills Acquired: Ability to apply co-design concepts in design flow for high-level specifications.

Course Contents

Unit 1: (15 hours)
Introduction to System Level Design - Generic Co-Design Methodology - Hardware Software Co-Design Models and Architectures - System Level Specification - Design and Modelling Languages.

Unit 2: (15 hours)
Design Representation for System Level Synthesis - Models of Computation - Architectural Selection - Partitioning - Scheduling and Communication - Model based Flows - Intelligent Partitioning Mechanisms.

Unit 3: (15 hours)
Hardware - Software Co-Simulation - FPGA Platforms - Gpus and Heterogeneous Platforms - Case Studies.

References

1. Patrick R. Schaumont, *A Practical Introduction to Hardware/Software Co-design*, Second Edition, Springer, 2013.
2. Jorgen Staunstrup and Wayne Wolf, *Hardware/Software Co-design: Principle and Practice*, Kluwer Academic Publishers, 1997.
3. Giovanni De Micheli, *Readings in Hardware Software Co-design*, Morgan Kaufmann, Academic Press, 2002.
4. Sao-Jie Chen, Kuang-Huei Lin, Pao-Ann Hsiung and Yu-Hen Hu, *Hardware Software Co-Design of a Multimedia SOC Platform*, Springer, 2010.

5. *Vivado Design Suite User Guide: Embedded Processor Hardware Design* UG898 (v2017.3) October 27, 2017.
6. ACM Transactions on Design Automation of Embedded Systems.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

Hardware Security and Trust

21VL734 **3-0-0-3**

Learning Objectives

LO1 To introduce security and trust issues associated with hardware systems.
LO2 To provide a background for recommending countermeasures for security and trust vulnerabilities.
LO3 To impart experience in the design and implementation of security and trust primitives on both ASIC and FPGA.
LO4 To impart knowledge aimed towards devising security and trust design and evaluation processes.

Course Outcomes

CO1 To understand various threats in Hardware systems due to hardware Trojans.
CO2 To apply various techniques to detect Hardware Trojans and securing designs.
CO3 To analyze various design for security methods.
CO4 To evaluate the requirements of reconfigurable hardware and security countermeasures.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	2	2
CO 2	-	-	2	2	-
CO 3	-	-	3	2	2
CO4	-	-	2	-	2

Skills Acquired: Will obtain a conceptual knowledge in securing VLSI hardware and design trusted hardware.

Course Contents

Unit 1: (15 hours)

Integrated Circuits (IC) Trojans - Vulnerabilities in Combinational and Sequential Logic - Trojan Taxonomy - Side-Channel Attacks include Power Spectrum Analysis - EM Analysis - Timing Analysis - System-Level Protection.

Unit 2: (15 hours)
Fault Injection and Attacks - FPGA Security Attacks - Physical Attacks on FPGA and Countermeasures - Physically Unclonable Functions (PUFs) - PUF Taxonomy – Delay Based PUFs on FPGAs - True Random Number Generators (TRNG).

Unit 3: (15 hours)
Countermeasures for Scan-based Attacks - Protection of Intellectual Property (IP) - Watermarking Techniques for IP Protection - Built-in Self-Authentication - Validation of Security and Trust.

References

1. M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust*, Springer, 2011.
2. Prabhat MishraSwarup BhuniaMark Tehranipoor, *Hardware IP Security and Trust*, Springer, 2017.
3. G. Edward Suh and S. Devadas, *Physical Unclonable Functions for Device Authentication and Secret Key Generation*, DAC-2007.
4. Badrignans, B., Danger, J.-L., Fischer, V., Gogniat, G., Torres, L. (Eds.), *Security Trends for FPGAs - From Secured to Secure Reconfigurable Systems*, Springer, 2011.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.

VLSI IoT

21VL735 **3-0-0-3**

Learning Objectives
LO1 To introduce IoT paradigm.
LO2 To impart knowledge of IoT building blocks and their interactions.
LO3 To provide exposure to typical approaches towards IoT VLSI system implementation.

Course Outcomes
CO1 Ability to understand the working of the Internet of Things.
CO2 Ability to develop IoT abstractions for real life problems.
CO3 Ability to identify building blocks for realizing IoT systems.

CO4 Ability to implement simple IoT systems in a VLSI platform.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	-	-	3	-	-
CO 2	-	-	3	-	2
CO 3	-	-	3	-	-
CO4	-	-	3	3	2

Skills Acquired: Design IoT solutions for applications by choosing appropriate VLSI platforms and design flows.

Course Contents

Unit 1: (15 hours)

Introduction to IoT - Features - IoT Stack - Technologies and IoT Challenges - Sensors and Hardware for IoT - Protocols.

Unit 2: (15 hours)

Model based Approaches - Hardware/Software Partitioning - Computing Paradigms/Platforms - IoT/Cloud Integration.

Unit 3: (15 hours)

Security aspects of IoT - Integrity - Confidentiality - Authenticity - Case Study of Design of a Typical IoT System.

References

1. Pethuru Raj and Anupama C. Raman, *The Internet of Things: Enabling Technologies, Platforms, and Use Cases*, CRC Press, 2017.
2. Adrian McEwen, *Designing the Internet of Things*, Wiley,2013.
3. Milan Milenkovic, *Internet of Things: Concepts and System Design*, Springer, 2020.
4. Cem Unsalan and Bora Tar, *Digital System Design with FPGA: Implementation Using Verilog and VHDL*, McGraw Hill,2017.
5. Journals and White papers.

Evaluation Pattern

Assessment	Internal	External
Periodical 1 (P1)	15	NA
Periodical 2 (P2)	15	NA
*Continuous Assessment (CA)	20	NA
End Semester	NA	50
Total	50	50

*CA - Can be Quizzes, Assignments, and Term Work with Report.