22EC801   VLSI Physical Design   3–0–1–4

1. Course Description

VLSI Physical Design has evolved as a complex specialization in VLSI and in-demand skill for the last 2 decades. VLSI Design cycle involves preparing the design for fabrication at a selected foundry (like TSMC, UMC, Global Foundries, etc.), with a specific technology node (like 90nm, 65nm, 45nm, etc.). This process involves several steps including synthesis, floor plan, power plan, placement, clock tree synthesis, routing, static timing analysis, timing optimization and ends with delivering GDSII files to the foundry after doing all sign-off checks. This course will give decent exposure to physical design concepts, techniques, along with hands-on labs using Cadence®/Synopsys®/Mentor Graphics® EDA tools.

2. Learning Objectives

(a) Analyse the basic flow (viz., full-custom/semi-custom) for VLSI physical design.

(b) Create partitioning, floorplanning, placement, routing and physical synthesis for integrated circuit (IC) chip.

(c) Analyse using the VLSI design automation tools to meet the power & timing constraints for an IC chip.

3. Course Outcomes

CO1 Create an overview of VLSI physical design flow.

CO2 Apply the VLSI EDA tools (both front-end & back-end) for IC chip design.

CO3 Apply the methods of placement and floorplanning and use the routing algorithms for compact integration.

CO4 Analyse the efficient clock distribution through the clock tree synthesis and create the physical layout for final tapeout.

4. Course Syllabus

Module-1 Introduction to VLSI Design flow, Physical Design Optimization, Electronic Design Automation (EDA) —Netlist & System partitioning, algorithms —Introduction to Floorplan & Floorplanning algorithms —Pin Assignment.

Module-2 Introduction to Placement, Optimization techniques, different approaches —Introduction to Routing viz., grid routing, global routing & their types, detailed routing & their related algorithms, power & ground routing —Basic concepts in clock networks, clock tree synthesis, clock routing.

Module-3 Introduction to Timing Closure, Timing Analysis & Performance Constraints, Timing-driven placement & routing —Introduction to performance–driven design flow, physical synthesis —Interconnect modeling, compact layout —Introduction to testing, fault modeling & simulation.

5. Textbooks

(a) Kahng, Andrew B., et al. *VLSI Physical Design: from Graph partitioning to Timing closure*. Springer Science & Business Media, 2011. ISBN-10: 9400790201, ISBN-13: 978-9400790209. Weblink

(b) Sait, Sadiq M., and Habib Youssef. *VLSI Physical Design Automation: Theory and Practice*. Vol. 6. World Scientific, 1999. ISBN-10: 9788175967342, ISBN-13: 978-8175967342. Weblink

References: (a) Online lectures. (b) Hands-on Tool tutorial

6. Weekly Plan

Week 1 : Introduction to physical design automation.

Week 2 : Partitioning, Floorplanning and Placement.

Week 3 : Grid Routing and Global Routing.

Week 4 : Detailed Routing and Clock Design.

Week 5 : Clock Routing and Power/Ground routing.

Week 6 : Static Timing Analysis and Timing Closure.

Week 7 : Physical Synthesis and Performance Driven Design Flow.

Week 8 : Interconnect Modeling and Layout Compaction.

Week 9 : Introduction to Testing, Fault Modeling and Simulation.

Week 10 : Test Pattern Generation, DFT and BIST.

Week 11 : Case Study - I: Physical design of some benchmark modules.

Week 12 : Case Study - II: Integration of the modules for a system design.

7. Evaluation Scheme

Components	Marks	
	Internal	*External*
Lab Assignments (40%)	40	NA
Continuous Assessment (30%)		NA
Project	20	NA
Paper Writing	10	NA
EndSem Written Exam. (30%)		30