FPGA-based network applications to simplify and transform your network infrastructure

Extensive Feature Set

- Data aggregation
- Precision time stamping
- Network monitoring
- Packet filtering
- Connection sharing
- Layer 2 switching
- Low-latency firewall

Ultra-Low Latency

- 39 ns multiplexing
- Multiplexing + filtering

Precision Monitoring

- High precision clock sync
- Precision time stamping
- Deep buffer capture aggregation

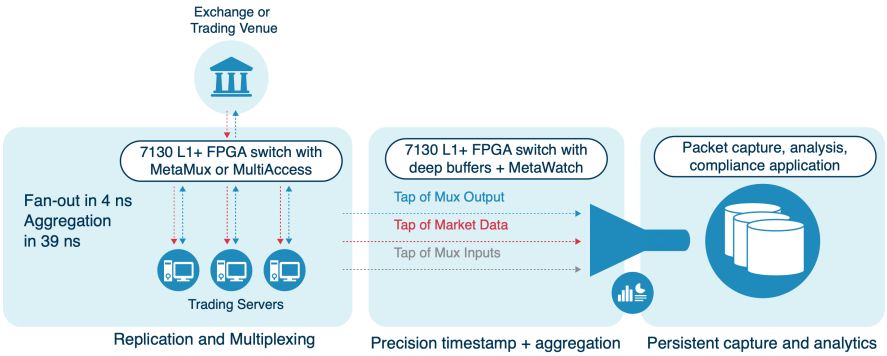
Custom Application Ready

- Develop and host your own apps
- Leverage prebuilt IP cores & toolkits

7130 Network Applications

Arista offers several powerful network applications to simplify and transform network infrastructure.

These applications are designed for use cases including ultra-low latency exchange trading, network visibility and providing vendor or broker-based shared services. Arista's 7130 supports these applications.



Financial services connectivity deployment example

The 7130 applications provided by Arista enable a complete lifecycle of packet replication, multiplexing, filtering, timestamping, Layer 2 switching, aggregation, and capture.

In addition to these application functions Arista also provides FPGA IP cores and development kits to enable companies to build their own custom applications.

Application	Key Features	Use it for …
MetaWatch **Advanced network monitoring**	• Regenerative tapping • Ubiquitous, lightweight tap aggregation • Multi-port data capture • Sub-nanosecond precise time stamping • Deep buffering (up to 32 GB)	• In-depth network monitoring and visibility • Improved network reliability & troubleshooting problems • Market data & packet capture • Accurate latency measurement & monitoring • Regulatory compliance (MiFID II - RTS 25)
MetaMux **Low-latency multiplexing**	• Data aggregation in 39 nanoseconds • Deterministic jitter • Packet statistics • BGP & PIM support	• Ultra-low latency network connectivity for trading • Market data fan-out and data aggregation for order entry at nanosecond levels

Application	Key Features	Use it for …
MultiAccess Connection sharing with enhanced security 	• Low-latency multiplexing and security • ACL-based configurable filtering • Easy to deploy data privacy for connection sharing • Simplified footprint for both mux and filtering applications • 10/1G Speed Conversion	• Secure network connection sharing • Providing sponsored access to multiple clients • Multi tenant exchange access • Low latency interconnect sharing • Supporting Colo deployments with multiple concurrent exchange connections
SwitchApp Low-latency Layer 2 Switching 	• 1/10/40G Layer 2 switching, implemented in FPGA • Ultra-low latency packet forwarding in 94 -132 ns • Full featured L2 switching pipeline powered by EOS • Non-blocking bandwidth profiles to provide up to 480 Gbps	• Multi-layer MLAG-based leaf-spine fabric, incl. redundant connections • L2 Multicast pub/sub • Supporting Colo deployments with multiple concurrent connections • Optimised distribution of traffic • Low latency back-office or message bus infrastructure
ExchangeApp Inline timestamping enables exchange fairness 	• Timestamp at the edge of trading venue networks • Sub-200ns passthrough latency to apply the timestamp • Reliable accuracy and timestamp precision • Accurately synchronise timestamps between multiple ExchangeApp devices	• Increase exchange fairness • Reduce trading venue latency sensitivity • Maintain trade order based on edge timestamps • Reduce complexity and risk of traditional low-latency exchange infrastructures
MetaProtect Firewall Low-latency packet filtering in 135 ns 	• Architected for ultra-low-latency with forwarding from 135 nanoseconds • Line rate 10GbE packet uni or bidirectional filtering between port-pairs • Stateless security policy with up to 510 rules per ACL • Full packet header logging for non-compliant packets	• Low-latency firewall • Satisfy InfoSec or regulatory compliance mandates without introducing excessive latency

Partner Ecosystem

Several tried & tested integrations exist via our technology partners. We enable our partners to deliver value and differentiation in a highly competitive marketplace. Joint innovation with our partners has proven to generate powerful complementary solutions that run on the 7130 platform and offer clients additional capabilities: optimized analytics, data capture solutions, and more.

Enabling Custom Applications

While FPGA applications can be challenging to develop, the Arista 7130 makes them easy to deploy. Arista provides a built-in application framework allowing developers to wrap applications into simple packages for deployment, streamlining operational processes. Arista development toolkits enable complete and unfettered access to the facilities provided by the in-system FPGAs. The MOSAPI provides monitoring, CLI, API, FPGA image management, and other facilities to allow application developers to concentrate on the core application functionality. EOS Support for application extensibility via EOSSDK will be implemented as a roadmap item.

Arista Development Kits

The Arista FPGA Development Kit (or Arista FDK):

The Arista FDK provides the documentation, libraries and examples which enable developers to build new FPGA applications running on Arista's 7130 platform. The development environment includes:

- Hardware documentation and information (currently supporting the 7130E, EH, L and LB development standards)
- IP Cores
- Working example applications, including example build systems
- Support resources to correctly build FPGA applications.

Note: The examples in the Arista FDK target the MOS operating system, and its MOSAPI SDK. As the 7130 Series transitions to EOS, these applications will transition to an enhanced EOS SDK. Please get in touch to discuss your specific SDK feature requirements. EOS application examples will be added in Q4, 2020.

Arista FDK IP Cores Support:

The Arista FDK includes all current Arista IP cores (FPGA libraries). These include:

- 10G MAC-PHY IP Core
- Mux IP Core
- TS IP Core

The Arista Switch Development Kit for Vitis™ :

Vitis is a powerful tool, designed by Xilinx, to better enable FPGA development. Vitis is designed to make it simpler to build FPGA applications using higher-level languages, reusable blocks, and a statically configured Vitis Target Platform in the FPGA. Arista provides support for Vitis development, via these Vitis Target Platforms which run on the LB development standard and support the many Ethernet interfaces provided by the **7130LB devices**. The Switch's internal CPU connects via PCIE to the FPGA, and supports XRT, giving a similar development experience to that of a server with an add-in PCIE card.

The Arista Switch Development Kit for Vitis provides:

- *MOS support for running Vitis target platforms. Arista's MOS includes Xilinx's XRT and its drivers*
- *A Vitis target platform for the FPGA in the Arista 7130 LB devices;*
- *An Arista app for managing the shells installed on a switch;*
- *An Arista 10GbE Ethernet kernel, including an example application using the Ethernet kernel;*
- *Example Vitis projects, including Xilinx's Market Maker example, and a software layer used to integrate this into the switch's operating system.*

Note: The Arista FPGA Development Kit for Vitis supports the MOS Operating System. Along with the Arista FDK, support for Arista's EOS will be added.

Arista IP Cores

Arista develops FPGA applications based on a mature base of network logic IP. To make it easier to develop compelling FPGA-based network applications, Arista licenses that IP as IP cores for use on the Arista 7130 platform. These are supported, proven building blocks that reduces time to implement your applications.

Core	Overview	Use it for …
10G MAC-PHY IP Core	An IP core for interfacing 10 gigabit Ethernet with low latency. • Implements a low latency Ethernet MAC and Physical layer (10GBASE-R) • Connects directly to FPGA top level serial transceiver pins and provides separate AXI4 interfaces for RX and TX user data • Supports Xilinx Virtex® 7, Xilinx Kintex® UltraScale™, and Virtex® UltraScale+™ FPGA's.	• Accelerating your own applications access to the 10G network
Mux IP Core	• Implements the same functionality as the Arista MetaMux application. • Allows for customisable radix and number of multiplexing cores e.g. one 4:1, plus a 13:1, plus a 14:1, etc	• Sharing the FPGA between the mux functionality and your own application • Building a multiplexing app with different configurations than the standard MetaMux application.
MMP IP Core	Provides a bus that leverages parallel I/O between FPGA's on the 7130 triple FPGA platforms. • 8 ns intra FPGA latency • Provides a low latency clock domain crossing FIFO • Supports four MMP links connecting each Leaf FPGA to the Central FPGA and two MMP links connecting the two Leaf FPGAs together	• The lowest latency , parallel communications bus for your multi FPGA applications • The fastest way to involve two FPGAs in a trading decision such as "splitting risk logic from trading logic".
Timestamp IP Core (TS IPCore)	Provides a timestamping and synchronisation engine, implemented as a combination of an encrypted RTL core, with a python based synchronisation daemon. When instantiated, the RTL core and software combination allows the system's OCXO to be synchronised to a PPS, PTP or NTP source. Multiple timestamper units can be instantiated to sample asynchronous strobes, providing nanosecond-precise timestamps within the RTL. The TS IP Core solution has the following specifications: • 1ns timestamp resolution with a +/- 2ns precision • Configurable triggering	• The lowest latency , parallel communications bus for your multi FPGA applications • The fastest way to involve two FPGAs in a trading decision such as "splitting risk logic from trading logic".