"CHIPS Metrology NOFO on Small Business Innovation Research (SBIR)" will begin at 3:30pmET.

Will the webinar be recorded?

- Yes, the webinar will be recorded, and both the recording and the slides will be available on the CHIPS R&D Funding Opportunities page here: https://www.nist.gov/chips/chips-rd-funding-opportunities.

Where can I find information on the NOFO being discussed today?

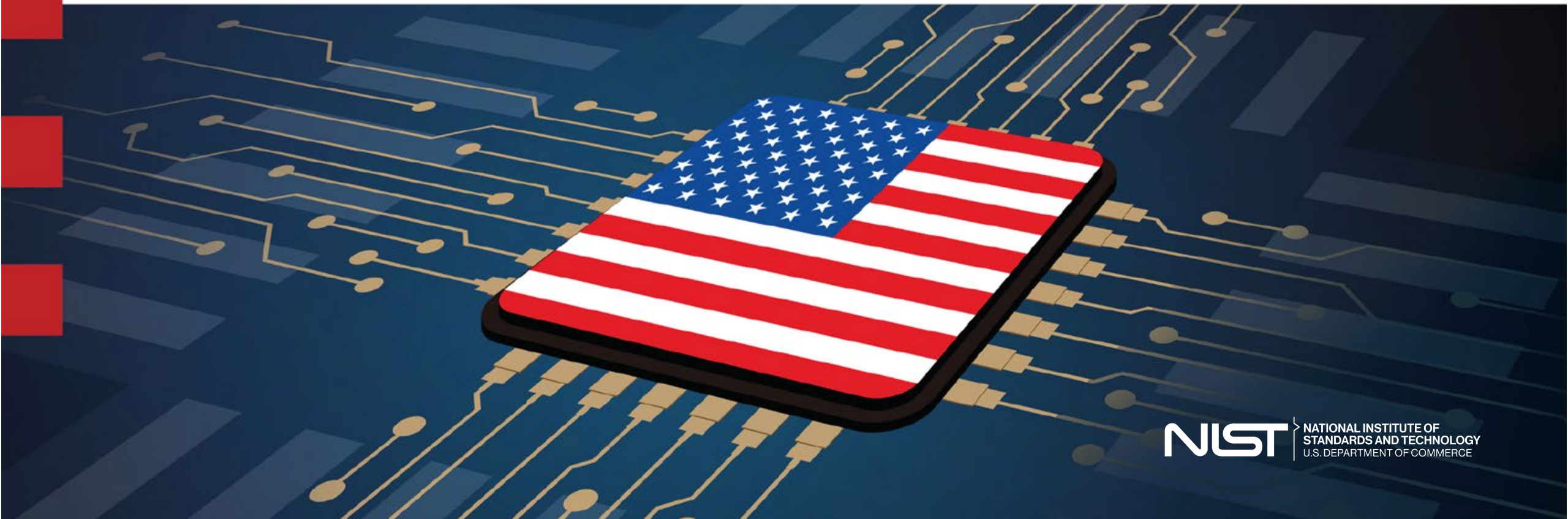
- Interested individuals can find the NOFO on grants.gov: grants.gov/search-results-detail/353574.

What if I have additional questions?

- If you have questions, please contact us at askchips@chips.gov.

CHIPS Metrology NOFO on Small Business Innovation Research (SBIR)

April 18, 2024



Disclaimer

- Certain commercial entities, equipment, or materials may be identified in this document in order to describe an experimental procedure or concept adequately.
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- Statements and responses to questions about advanced microelectronics research and development programs in this webinar:
  - Are information, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on the National Institute of Standards and Technology or the Department of Commerce.
  - Are subject in their entirety to any final action by the National Institute of Standards and Technology or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

Today's Speakers

Marla Dowell

Director, CHIPS
Metrology Program

Sarah Hughes

Chief of Staff, CHIPS
Metrology Program

Dean Iwasaki

Grants Officer and
Team Lead, NIST

Agenda and Objectives

Agenda

- Introduction to the CHIPS Research & Development (R&D) Office
- Small Business Innovation Research (SBIR) Program and CHIPS Metrology Notice of Funding Opportunity (NOFO) Overview
- Application Process
- CHIPS Metrology NOFO Application Topics
- Next Steps and Additional Resources

By the end, attendees should better understand:

- Vision for Success for the CHIPS Metrology NOFO
- Topics this NOFO will address
- How to submit an application in response to this NOFO

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Introduction to the CHIPS Research and Development (R&D) Office

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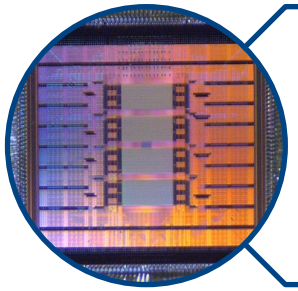
U.S. DEPARTMENT OF COMMERCE

2030 Goals



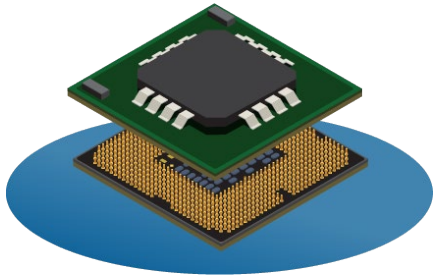
U.S. technology leadership

Accelerate ideas to market

A robust semiconductor workforce

CHIPS R&D Programs

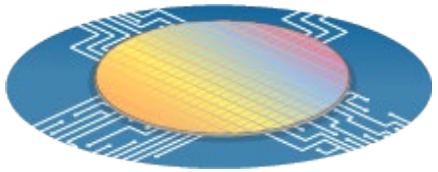
CHIPS Metrology Program



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program

Workforce Initiatives

CHIPS Metrology

VISION:

CHIPS Metrology catalyzes innovation with an emphasis on accurate, precise, and fit-for-purpose measurements for producing microelectronic materials, devices, circuits, and systems.

MISSION:

Measure, innovate, and lead to enhance a vibrant U.S. ecosystem for semiconductor manufacturing and to promote U.S. innovation and industrial competitiveness.

GOALS:

1. Expanding measurement solutions for the semiconductor ecosystem.
2. Increase the number of solvers by harnessing the diversity of people and ideas, inside and outside of NIST.
3. Expand education and workforce development opportunities that inspire excitement about manufacturing careers and expand career pathways.

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SBIR Program and CHIPS Metrology NOFO Overview

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What is the SBIR Program?

- Encourage domestic small businesses to **engage in research and development (R&D)** with the **potential for commercialization.**
  - Stimulate commercialization of technological innovation from the private sector through Federal R&D funding.
  - Foster participation in innovation by **socially and economically disadvantaged small businesses.**
- Federal agencies with extramural R&D budgets exceeding $100 million are required to participate.
  - Agencies determine R&D topics in their solicitation or **Notice of Funding Opportunity (NOFO)**.
  - Awards made after proposal evaluation.
  - Application requirements vary depending on agency.

Eligibility

Small Business Concern

- ✓ For-profit business **located in the United States**
  - Primarily operates within the United States, or makes significant contribution to the United States economy
- ✓ **For-profit business** structured as an individual proprietorship, partnership, limited liability company, corporation, joint venture, association, trust, or cooperative
- ✓ **More than 50% of equity owned and controlled by:**
  - One or more individuals who are United States citizens or permanent residents
  - Other for-profit small business concerns also owned and controlled by either U.S. citizens or permanent residents
  - Combination of the two above
- ✓ **No more than 500 employees,** including affiliates

SBIR Program Phases

	Purpose	Description	Duration
Phase I	Feasibility	Awardees establish the technical merit, feasibility, and commercial potential of their proposed efforts.	6 months
Phase II	Research and Development	Awardees are subjected to a technical review and evaluation process of Phase I efforts to determine if eligible for Phase II funding. If awarded, awardees continue the work conducted during Phase I.	2 years
Phase III	Commercialization	Small businesses pursue commercialization objectives from Phase I and II activities. SBIR programs do not fund Phase III.	No limit (non-SBIR funds)

FY24 SBIR CHIPS Award Information

Number of Awards

- **Open Topic Proposals:** up to 2 funding awards per Grand Challenge
- **Closed Topic Proposals:** up to 10 funding awards total
- Funding opportunity is a cooperative agreement (grant), not a contract

Funding Amounts

- **Phase I:** Up to $283,500, with an additional $6,500 for Technical and Business Assistance
- **Phase II:** Up to $1,910,000 with up to $50,000 for Technical and Business Assistance

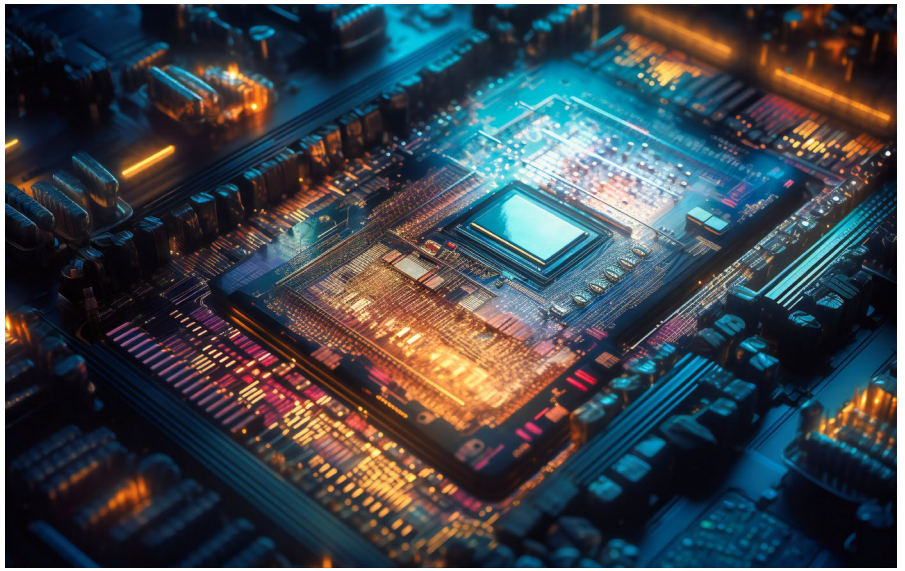
Period of Performance

- **Phase I:** 6 months, with one month allocated after to prepare and submit a final report for Phase II funding consideration
- **Phase II:** Up to 24 months

Technical and Business Assistance (TABA)

- Funding opportunity included in SBIR award to help small businesses commercialize their technology, by either:
  - Funding vendors directly, or
  - Providing funds to the small business awardees to contract their own vendors or consultants.

- NOFO has more details on how and when awardees can apply for TABA.



Important Dates

APRIL 16, 2024

CHIPS Metrology NOFO posted on Grants.gov.

JUNE 14, 2024

Full applications must be received at Grants.gov ***no later than*** 11:59 p.m. Eastern Time.

Applications received after this deadline will not be considered.

JUNE – AUGUST 2024

NIST application review, selection, and award processing take place.

SEPTEMBER 2024

Anticipated earliest start date for awards under this NOFO.

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Application Process

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Registration Requirements

System for Award Management (SAM.gov)

- Organizations must register with both SAM.gov and Grants.gov to apply.
- Receive Unique Entity ID (UEI), a 12-character alphanumeric ID assigned to an entity.
- SAM.gov registration process can take up to ten days.

Small Business Administration (SBA) Company Registry Form (SBIR.gov)

- Tracks ownership and affiliation requirements for all companies applying to the SBIR program.
- Each applicant must register in the Company Registry prior to applying.
- Completed registration documents required in application (NOFO section 8.02)

Grants.gov

- All applications will be submitted through Grants.gov.
- Applicants should visit Grants.gov for information on any scheduled closures for routine maintenance.
- Large files take several minutes to upload into Grants.gov.

All applications due ***no later than*** 11:59 p.m. Eastern Time on **June 14, 2024.**

Application Options

Fast-Track

- Submit both Phase I and Phase II technical approaches in application.
- Minimize funding gaps between phases.
- Requires fully developed Phase II approach at the time of submission.

Phase II

- Successfully completed previous Phase I funding from either NIST or a different agency.
- Topic relates to one of the closed topics identified in the NOFO.
- Submit “final report” from Phase I funding and fully developed Phase II application.

Full Application Requirements

Section	Additional Details	Page in NOFO
SF-424 (R&R), Application for Federal Assistance	The SF-424 (R&R) must be signed by an authorized representative of the applicant's organization.	Pg. 71
Research and Related Budget	This includes total Federal amount requested.	Pg. 71
CD-511, Certification Regarding Lobbying Activities	Only include in application if applicable.	Pg. 72
Research and Related Other Project Information	Please attach a document to field 7 stating, "A Project Summary/Abstract is not relevant to this competition".	Pg. 72
SF-LLL, Disclosure of Lobbying Activities	If applicable.	Pg. 72
Technical Content: Cover Sheet & Proposal	The Technical Content must not exceed 15 pages including optional letters of support	Appendix A – Cover Sheet & Section 3
Budget Narrative and Justification	A written justification should include the necessity and the basis for the cost.	Pg. 73
Indirect Cost Rate Agreement		Pg. 75

Nothing listed supersedes NOFO.

Full Application Requirements *(continued)*

Section	Additional Details	Page in NOFO
SBA Company Registry Form	Company Registry to track ownership and affiliation requirements for all companies applying to the SBIR	Pg. 75
Data Management Plan (DMP)	The DMP must include, at a minimum, a summary of proposed activities that are expected to generate data	Pg. 75-76
Subaward Budget Form	Required if sub-recipients and contractors are included in the application budget.	Pg. 76
Research & Related Personal Data	Form is available in the R&R Family section of Grants.gov. Complete the form and attach a PDF copy.	Pg. 76
Current and Pending Support Form	Identify all sources of current and potential funding, including this proposal.	Pg. 77
Compliance with SBIR Program Requirements, Applicant Fraud Awareness Training – Certification of Training Completion	Complete the training at: https://www.nist.gov/file/384881. After completion, print and fill out the last page of the training presentation.	Pg. 77
Letters of Commitment	Letters of Commitment must be signed by an individual with authority to legally bind the organization to its commitment.	Pg. 77
Company Commercialization Report (CCR)	Attach a PDF copy of the CCR which was completed in your account at Sbir.gov	Pg. 78
Required Disclosure or Relationships to Foreign Countries	Attach a PDF copy of the completed signed and dated Appendix C disclosure form	Appendix C

Nothing listed supersedes NOFO.

Important Dates

APRIL 16, 2024

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SEPTEMBER 2024

Anticipated earliest start date for awards under this NOFO.

Application Evaluation Criteria

- ✓ Proposed technical approach is comprehensive, feasible, and demonstrates a clear understanding of the research area **(20 points).**
- ✓ Appropriateness of qualifications and extent of the experience of the proposed principal/key investigators, supporting, staff, and consultants as they relate to accomplishing the proposed research effort. The extent to which the applicant can access the necessary facilities and equipment to complete the proposed research **(5 points).**
- ✓ Likelihood the proposed research program will lead to a successful product or service with a viable pathway for commercial deployment as described **(30 points).**
- ✓ Magnitude of the anticipated commercial benefits of the resulting product or service **(25 points).**
- ✓ Extent to which the proposed commercial product or service enhances U.S. economic or national security competitiveness and relates to and advances the CHIPS Metrology Program's goals and mission **(20 points).**

Nothing listed supersedes NOFO.

For more information, please reference page 47 in the NOFO.

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CHIPS Metrology NOFO Application Topics

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CHIPS Metrology Grand Challenges

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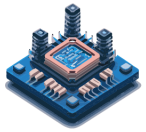
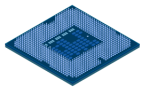
GC4 - Modeling and Simulating Semiconductor Materials, Devices, and Components

Design Metrology
Material and device models; physical metrology

Circuit Design
Integrated circuits (IC), systems intregration



Mask Design
Template for the IC



GC5 - Modeling and Simulating Semiconductor Manufacturing Processes

Wafer Fabrication
Deposit a film, pattern a photoresist (litho), use as a stencil to etch the film

Deposition
Metal, dielectric

Lithography
Photoresist spin coat, expose, and develop

Etching
Heat/bake, etch, and remove resist

GC1 - Materials Purity, Properties, and Provenance

Materials Quality Metrology
Acceptance inspection and testing for defects, purity, and other properties

Materials Supply
Over 800 diverse materials

GC2 - Advanced Metrology for Future Manufacturing

Fab Metrology
In-line metrology; inspection for defects; wafer and thin film quality inspection; mechanical testing, density and surface charge analysis; dimensional analysis of fine patterns and contact hole diameters

Repeat 40 –100 times

GC3 - Metrology for Advanced Packaging

Wafer/Package Metrology
In-line metrology; inspection and testing for accuracy and precision of performance; patterned wafer inspection for defects; quality inspection of packaging performance

Testing

Wafer Test
Each die individually tested on wafer

Packaging

Assembly/Integration
Wafer dice, sorting, die attach, bonding

Testing

Test Packages
Final product testing

End Products

Integration
Chips integrated in end products (OEMs)

Cross Cutting

GC6 - Standardizing New Materials, Processes, and Equipment

GC7 - Security and Provenance of Microelectric Components and Products

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

Open and Closed Topics

Open Topics (7 Total)

- Topic areas focused on addressing the CHIPS Metrology Grand Challenges, sourced by industry.
- Small businesses share how their work aligns with a Grand Challenge and how they will conduct R&D to address the Path Forward Element for that Grand Challenge.
- Looking for innovation from companies.

Closed Topics (10 Total)

- Topic areas focused on addressing identified needs from CHIPS Metrology-funded projects aligned with specific Grand Challenges.
- Small businesses share how their work aligns with the requested topic area/need and how it will work collaboratively with the project team to help advance R&D.
- Looking to address that specific topic area/need in the technical approach.

Open Topics: Path Forward Elements (Section 9.1)

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GC1 - Materials Purity, Properties, and Provenance

Conduct high-impact R&D and related activities in critical areas including new measurements with increased sensitivity and throughput, and Standard Reference Materials (SRMs). **[Page 81 in NOFO]**

GC2 - Advanced Metrology for Future Manufacturing

Conduct activities in critical areas to develop innovative, cost-effective metrology applicable to 3D device and next-generation manufacturing. **[Page 81 in NOFO]**

GC3 - Metrology for Advanced Packaging

Conduct R&D to develop metrology to address the unique challenges presented by advanced packaging, including subsurface features and aspects related to heterogeneous integration. **[Page 82 in NOFO]**

GC4 - Modeling and Simulating Semiconductor Materials, Devices, and Components

Conduct R&D to develop robust data, mathematical models, and measurement techniques for important future device parameters that are needed to support effective design simulators. **[Page 83 in NOFO]**

GC5 - Modeling and Simulating Semiconductor Manufacturing Processes

Conduct R&D to develop a variety of effective manufacturing simulation tools and related standards that can be applied to in-line processes and model key parameters. **[Page 83 in NOFO]**

GC6 - Standardizing New Materials, Processes, and Equipment

Conduct R&D, data collection, process validation, and other standards activities to support the development of documentary standards, SRMs, and calibration protocols for semiconductor manufacturing. **[Page 84 in NOFO]**

GC7 - Security and Provenance of Microelectric Components and Products

Conduct activities to support the development of standards, protocols, and testing processes for analyzing security vulnerabilities in microelectronics across their entire life cycle. **[Page 84 in NOFO]**

To learn about the specific R&D and related activities for each Grand Challenge's Path Forward Element within the NOFO, please reference Section 9.1 of the NOFO.

Closed Topics: Project-Specific Need

Topic	Page in NOFO
Topic 1: Near-Real Time RF Propagation Measurement System	Pg. 85
Topic 2: Compact, fieldable cryogenics for deployment of superconducting-nanowire single-photon detectors in a circuit-evaluation microscope	Pg. 86
Topic 3: Microscope for time-resolved emission microscopy with superconducting-nanowire single-photon detectors	Pg. 87
Topic 4: Device-Scale AFM-Thermoreflectance Hybrid Metrology	Pg. 88
Topic 5: Super-resolution beam scanning, wide bandwidth, optical photothermal infrared (O-PTIR) microscope	Pg. 90
Topic 6: High brightness compact X-ray or EUV sources for semiconductor metrology	Pg. 92
Topic 7: Nanoscale dimensional metrology reference standards to support semiconductor metrology	Pg. 93
Topic 8: Advanced Electron Backscatter Diffraction (EBSD) detector offering high pixel density, high-speed and low noise operation, and low kV detection enabled by directly detecting electrons using an application specific integrated circuit (ASIC) detector	Pg. 94
Topic 9: TEM High Voltage Biasing Holder	Pg. 96
Topic 10: Wafer-scale ferromagnetic resonance spectrometer for Advanced MRAM Wafer Data and Quality Control	Pg. 97

Closed Topic Example

Field	Example Text	Page in NOFO
Title	Compact, fieldable cryogenics for deployment of superconducting-nanowire single-photon detectors in a circuit-evaluation microscope	Pg. 86
Scope Description (with technical requirements)	Superconducting-nanowire single-photon detectors offer excellent performance for measuring the faint photonic emission from transistors. Utilizing these detectors in a field analysis lab at a semiconductor development company requires deployment of cryostats to operate in a microscopy apparatus with minimal maintenance and cryogenic expertise required by the laboratory technician. The anticipated commercial outcome of this innovation is a compact cryostat for cooling small sensors and/or samples ... with the following requirements set: • The cryostat must reach a base temperature of 2.3K • It must not require replenishment of liquid cryogens (Please see continued description and technical requirements in NOFO)	Pg. 86-87
Desired Objectives & Outputs per Phase I	Outputs: Analysis & Prototype A final report detailing the design of the cryostat that meets the above requirements set, including the choice of pulse tube based on required cooling power, the design of the low-temperature stage accommodating the focal plane array, the optical path, with low-temperature focusing optics, the cryogenic amplifiers on the 4K stage, the micro-coax wiring going to 300K, and the design of the optical and mechanical mating to the microscope.	Pg. 87
Desired Objectives & Outputs per Phase II	Output: Hardware A fully functional version of this cryostat meeting all the above specifications, capable of mating to the microscope.	Pg. 87

Nothing listed supersedes NOFO.

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Next Steps and Additional Resources

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Next Steps

- Verify your small business is eligible and complete all registration requirements.
- Determine which application option applies to your business.
- Download the NOFO and Look at Section 1.04 (pg. 17), Contact with NIST, to address any questions.
- Review the open and closed topic areas.
- Draft your application, ensuring all required sections are completed and identified needs are addressed.
- Apply via Grants.gov by **11:59 p.m. Eastern Time on June 14, 2024.** Give yourself ample time to complete the application.

Resources

- **SBIR page:** https://www.sbir.gov/
- **SBA Company Registration:** https://www.sbir.gov/registration

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- **2024-SBIR-CHIPS-01 NOFO link:** grants.gov/search-results-detail/353574
- **NIST SBIR page:** https://www.nist.gov/tpo/small-business-innovation-research-program-sbir
- **NIST SBIR Frequently Asked Questions (FAQs):** https://www.nist.gov/tpo/small-business-innovation-research-program-sbir/resources/notice-funding-opportunity-nofo-faqs
- **CHIPS R&D Funding Opportunities page:** https://www.nist.gov/chips/chips-rd-funding-opportunities
- **CHIPS Metrology Program page:** https://www.nist.gov/chips/research-development-programs/metrology-program
- **Strategic Opportunities in U.S. Semiconductor Manufacturing:** https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

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Thank You!

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