April 2021 · Jan-Peter Kleinhans

The lack of semiconductor manufacturing in Europe

Why the 2nm fab is a bad investment.

Stiftung Neue Verantwortung

Think Tank at the Intersection of Technology and Society

Executive Summary

As part of the *2030 Digital Compass* decadal plan, the European Commission aims to establish cutting-edge semiconductor manufacturing in the European Union (EU). The goal is to operate semiconductor fabrication plants (fabs) with 2nm process nodes within the EU by the end of this decade. This would require tens of billions of Euros in public and private investment. To make this investment strategically sound in the long-term, such an "EU foundry" must have a solid business case based on substantial demand in the market, especially in the highly competitive market of cutting-edge chip manufacturing which has almost insurmountable barriers to entry. Unfortunately, chasing the 2nm fab is a futile endeavor with a very real risk of wasting billions of Euros in public and private money. This idea lacks a business case due to the following factors.

First, an EU foundry would predominantly serve European customers, but there are very few semiconductor companies in the EU designing chips on 7nm or 5nm nodes today. Most types of chips that Europe's leading semiconductor companies produce do not benefit from cutting-edge manufacturing. Thus, companies did not invest in cutting-edge fabs for almost two decades. This lack of cutting-edge chip designs in the EU directly translates into miniscule demand for cutting-edge contract chip manufacturing. Therefore, before investing in supply (creating cutting-edge fabs), Europe needs to create demand by investing substantially in its own chip design capabilities.

Second, it is at best overly optimistic and at worst naïve to hope an EU foundry would attract orders from US chip design companies. It is highly likely that the two companies at the forefront of cutting-edge chip manufacturing, TSMC in Taiwan and Samsung in South Korea, will establish advanced fabs in the United States. Not least because the United States has the largest chip design industry by far. Thus, to alleviate national security and business continuity risks, within the next three to four years US fabless companies will be able to order advanced chips from TSMC's and Samsung's US foundries. This outlook further deludes the unique selling point of an EU foundry. What is the rationale for a US fabless company to order chips from TSMC EU rather than from TSMC Taiwan or TSMC US?

Third, it is not by chance that the market for cutting-edge chips manufacturing consolidated substantially over the last 20 years: Skyrocketing investment costs for fabs and the need for extensive R&D collaborations across the entire supply chain to advance the cutting-edge, all while maintaining high utilization rates to amortize equipment costs within a few years, led to most companies dropping out of "More Moore Scaling." Only two companies operate cutting-edge fabs: Samsung in South Korea and TSMC in Taiwan.

Even if Europe were able to set up an advanced fab through a concerted effort and tens of billions of Euros of private and public money, this money and resources would be better spent in other areas where Europe is even more dependent on foreign technology providers: designing cutting-edge logic chips (such as processors for data centers, high-performance computing, artificial intelligence and mobile applications). Europe's Achilles heel is the lack of fabless companies that design chips. Once Europe's chip design prowess is rejuvenated, the region will be in a much stronger position to think about how best to invest in its manufacturing capabilities.

Table of Contents

SNV's Technology and Geopolitics project was made possible by the generous support of (in alphabetical order) the *Dutch Ministry of Economic Affairs and Climate Policy*, the *Finnish National Emergency Supply Agency*, the *Finnish Ministry for Foreign Affairs*, the *German Federal Foreign Office* and the *Swedish Ministry for Foreign Affairs*. The views expressed in this paper do not necessarily represent the official positions of these ministries.

Introduction

The semiconductor industry has received considerable attention from policy makers in recent years. Governments increasingly perceive semiconductors as strategic assets where technology leadership must be achieved to strengthen economic and national security. Thus, "chips" are at the heart of the intensifying technology rivalry between the United States and China.[1] The US government is especially worried about the industry's dependence on foreign semiconductor manufacturing. Although all over the world the number of companies designing their own chips is increasing, today significantly fewer companies operate cutting-edge fabrication plants ("fabs" with ≥7nm process nodes) to manufacture the chips than 20 years ago.[2] Cutting-edge wafer fabrication, the manufacturing of semiconductors, is a highly concentrated market in terms of companies and geography. Currently, only TSMC in Taiwan and Samsung in South Korea successfully operate cutting-edge process nodes at 7nm and below, which are necessary for many modern logic semiconductors, such as processors in consumer electronics, laptops and data centers. Not surprisingly, the US government wants to reduce the country's dependence on foreign technology providers and strengthen its own semiconductor manufacturing base through various industrial policies.[3]

In a similar move, the European Union identified semiconductors as a prerequisite for its own "technological sovereignty". Although there have been previous efforts to strengthen the EU's semiconductor industry and gain market share, they were not hugely successful. For the past three decades, the global market share of the EU's semiconductor industry was around 10%.[4] Not least because of the US-China technology rivalry, rising geopolitical tensions and increasing scrutiny of global supply chains due to COVID-19, discussions about how to rejuvenate the EU's semiconductor prowess are resurfacing. In December 2020, the majority of EU member states signed a joint declaration, titled *A European Initiative on Processors and Semiconductor Technologies*,[5] with the goal to substantially invest in the EU's semiconductor industry. In the *2030 Digital Compass*, the European Commission defined its decadal ambition: a 20% market share and establishment of cutting-edge fabs with <5nm process nodes.[6] The *2030 Digital Compass*, the joint declaration and the broader policy discussions[7] consistently mention the lack of advanced wafer fabrication as the EU's central weakness regarding semiconductors.

This paper argues that the strong focus on establishing cutting-edge fabs in the EU is ill-advised and the wrong first step to meaningfully strengthen the EU's semiconductor industry. To make that point, this paper analyzes the role of wafer fabrication in the semiconductor value chain. Then, the paper identifies why the market for cutting-edge fabs is highly concentrated and why there are no cutting-edge fabs in the EU. Last, this paper argues that there is no business case for an advanced fab in the

EU, and that the lack of advanced logic chip design is the EU's Achilles heel. Before thinking about advanced logic fabs, the EU must invest substantially in its own advanced logic chip design capabilities.

To get the most out of this paper, it is highly recommended to read SNV's first analysis from October 2020, "The Global Semiconductor Value Chain: A Technology Primer for Policy Makers."[8] It provides an overview of the semiconductor production stack and explains the different business models, important regions, interdependencies as well as choke points.

1. The economics of advanced wafer fabrication

The fab is where everything comes together. Whether operated by an integrated device manufacturer (IDM), such as Intel, or a foundry, such as TSMC, fabs rely on a highly specialized and complex supply chain. Establishing such an ecosystem is hard and easily takes more than a decade.

Foundries have to collaborate closely with fabless companies that must base their chip design on a specific process node. Fabs work closely with electronic design automation (EDA) tool vendors to develop new process nodes and ensure that the EDA software supports the fab's process nodes.[9] Fabs also have close ties with equipment, chemical and wafer vendors. For example, several Taiwanese chemical suppliers plan to move with TSMC to Arizona in the US to support the company's new fab.[10] In 2020, ASML established a training center in Taiwan, next to TSMC, to train engineers for 18 months on ASML's complex photolithography equipment, necessary for process nodes below 7nm.[11] In addition to these close business relationships, fabs maintain a multitude of R&D collaborations with research and technology organizations (RTOs), EDA, equipment and chemical suppliers to develop the next generation of process nodes.

Additionally, fabs that depend on "node shrinkage" typically work on several process nodes at the same time. TSMC's 5nm process nodes are currently in "volume production," but the company plans to start "risk production" on its 3nm nodes in 2021 and is already researching process nodes of 2nm and below.[12] This node shrinkage or "More Moore Scaling" (more transistors per square millimeter with better performance, less power consumption and lower costs) is especially important for logic semiconductors in the consumer market, such as processors in smartphones and laptops.[13] At the same time, this market segment generates the high volumes that make the enormous upfront investments in chip design and manufacturing economically viable[14]: For example, Apple's iPhone sales totaled US$65.6 billion in 4Q 2020 alone.[15] With that amount of quarterly sales, Apple can afford to invest billions in its own chip design and contract with TSMC to manufacture the chips. Because of these economies of scale, the most advanced chips in terms of "PPAC" (power, performance, area, cost) are found in consumer electronics.

That said, many types of semiconductors, such as analog and mixed-signal semiconductors (power supply and radio frequency (RF) chips, sensors and many more), do not depend on node shrinkage. Therefore, comparing fabs from Texas Instruments, Analog Devices or Infineon[16] (several of the leading analog semiconductor companies) with fabs from Intel, Samsung or TSMC is comparing apples and pears.

How the era of "More Moore Scaling" led to substantial fab consolidation

Samsung in South Korea and TSMC in Taiwan are at the forefront of "More Moore Scaling" and mastered node shrinkage. Because it depends heavily on economies of scale, it is not surprising that Samsung and TSMC are also the leaders in wafer capacity (the number of silicon wafers run through their fabs each month). Each company has a higher wafer capacity than all the fabs in the United States added together.[17] Although there are more than 10 foundries in the world with process nodes of 40nm and higher, only Samsung and TSMC successfully operate nodes at 7nm and below.[18] This also means that currently, any wafer capacity below 10nm is available only in South Korea or Taiwan (see figure 2). However, this may change within 3 to 5 years, as TSMC and Samsung plan to build relatively cutting-edge fabs in the United States.[19]

Looking at the business dynamics, it was inevitable that over the last 20 years most companies would drop out of "More Moore Scaling." To better understand this development, three factors must be considered: skyrocketing investment costs for cutting-edge fabs, increasing R&D intensiveness across the entire supply chain and necessarily high fab utilization rates to amortize the capital expenditure.

- **Skyrocketing costs of new fabs:** Capital expenditure for a modern (5nm) fab is close to US$20 billion with annual operating expenditures of more than US$1 billion.[20] The skyrocketing costs mainly stem from increasingly complex and expensive manufacturing equipment.[21] Part of the rising operating expenditures are electricity costs. For example, analysts estimated that TSMC accounted for close to 5% of Taiwan's electricity consumption in 2019.[22]

- **High volume, high utilization:** To amortize such a huge investment within a few years, a fab needs high utilization rates. UMC, the second largest foundry in Taiwan, had quarterly utilization rates of 93–99% in 2020.[23] Some analysts expect that Samsung's and TSMC's 7nm nodes will have utilization rates of 95–100% in 2021.[24] There is essentially no "spare capacity" in wafer fabrication, especially not at the cutting-edge. Fabs simply cannot afford it.

- **Increasing complexity and R&D intensiveness:** Advanced logic fabs are more than just expensive equipment in gigantic cleanrooms. Ensuring rapid time to market, high yield rates (the percentage of "good" chips on a wafer after fabrication) and high utilization rates, all at the same time, requires substantial process knowledge and managerial skills.[25] Moreover, fabs need to advance node shrinkage through substantial R&D collaborations to develop future process nodes.[26]

With these economics at play, it is not surprising that only a few companies in the world have the expertise, money and ecosystem to successfully operate cutting-edge fabs. Contract manufacturing below 10nm is down to Samsung and TSMC. Intel fell behind, but even if they manage to catch up with TSMC and Samsung, as an IDM Intel so far built fabs for its own production and thus, does not provide wafer capacity to the market.[27] The company announced to offer foundry services in the future[28] but it will take many years, if successful at all.[29] Last, even if the US administration in the future reduces the export restrictions against SMIC, the largest Chinese foundry and only contender focused on "More Moore Scaling," it is unclear whether SMIC will be able to successfully operate 7nm nodes within three to five years.[30]

"More Moore Scaling" will most likely continue for another 10–15 years,[31] and its economics have created insurmountable barriers to entry. Thus, it is quite likely that the industry will continue to rely solely on TSMC and Samsung for cutting-edge wafer fabrication.

2. Why the EU has no cutting-edge fabs

Assessing the technological advancement of a fab based only on the "nanometers" of its manufacturing process poses some problems. First, for many years the number of nanometers has not described any actual physical dimension of the final integrated circuit or the fabrication process: "14nm" and "7nm" are merely marketing terms. They can be used as a general indicator but not as much more.[32] Second, process node density is mostly relevant for logic semiconductors: A processor manufactured on a 7nm node consumes less energy and thus, can be more complex and powerful than a processor manufactured on a 28nm node. However, node density is not a relevant measure for many other types of semiconductors, such as analog semiconductors and sensors. Innovation in analog and mixed-signal semiconductors, such as power supply chips or radio frequency applications, is driven by utilizing new materials, such as silicon-carbide (SiC) or gallium-nitride (GaN), instead of node shrinkage. In addition, modern analog fabs cost several times less than cutting-edge fabs for logic or memory chips.[33]

That said, when looking at wafer fabrication in Europe (not just the EU), it becomes clear that there is a severe lack of advanced logic fabs. Furthermore, compared to China, Japan, South Korea, Taiwan and the United States, Europe has by far the smallest overall wafer capacity, no matter the technology node. The following chart (**figure 1**) shows the total wafer capacity per region for 2010, 2015 and 2020. Although Europe has the smallest wafer capacity today, the region also grew its wafer capacity by only 18% over the past 10 years, in stark contrast to China (+205%), South Korea (+126%) and Taiwan (+67%).

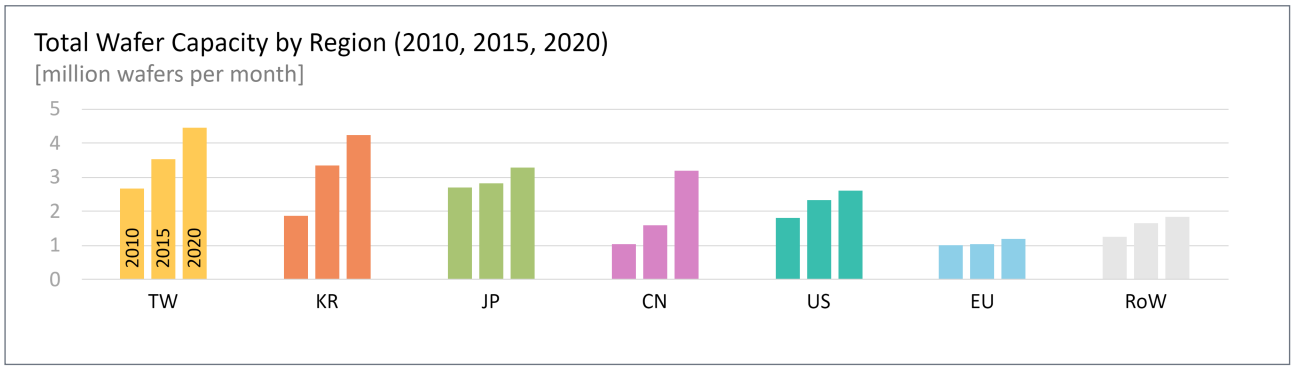

Figure 1

Looking at regional wafer capacity for specific technology nodes (**figure 2**), it is obvious that cutting-edge wafer fabrication at 7nm or less takes place only in South Korea and Taiwan. However, more importantly, Europe lacks cutting-edge *as well as* trailing-edge (a few generations behind the cutting-edge generation) logic fabs:

- **<20nm to ≥10nm**
  The tiny share of wafer capacity for ≥10nm to <20nm process nodes is almost entirely due to Intel's fabs in Ireland (14nm) and Israel (10nm).[34] Currently, no foundry in the EU has these trailing-edge nodes. So far, Intel utilizes these fabs for its own production, and they are not available to the market for contract manufacturing. This might change in the future if Intel decides to offer its foundry services in its Ireland fabs.[35]

- **<40nm to ≥20nm**
  In addition to Intel's fabs with process nodes of <40nm to ≥20nm in Ireland and Israel, there are fabs from STMicroelectronics in Crolles, France[36] (28nm FD-SOI[37]), and Globalfoundries in Dresden, Germany[38] (22nm FD-SOI). Globalfoundries, headquartered in the US but owned by a state-owned investment company from the United Arab Emirates, the only trailing-edge foundry in EU.

- **<180nm to ≥40nm**
  Many European IDMs operate these "mature" nodes in the EU. In addition to STMicroelectronics in France and Italy, and Globalfoundries in Germany, Bosch (≥65nm in Dresden, Germany),[39] Infineon (≥90nm in Dresden, Germany),[40] X-FAB (≥130nm in Corbeil-Essonnes, France) and NXP (≥140nm in Nijmegen, the Netherlands)[41] operate these process nodes. Although some of these nodes could be considered "antique" by today's standards for mobile chips and processors, the nodes are in high demand for chips in automotive and industrial applications.

- **≥180nm**
  Almost 50% of Europe's total wafer capacity consists of nodes that are 180nm or larger. Although they were introduced more than 20 years ago, these nodes are still in use today for power semiconductors, sensors and other types of analog semiconductors. In addition to the companies above, many specialty foundries such as X-FAB[42] and United Monolithic Semiconductor (UMS)[43], both with fabs in Germany and France, operate process nodes with densities of 180nm and higher.

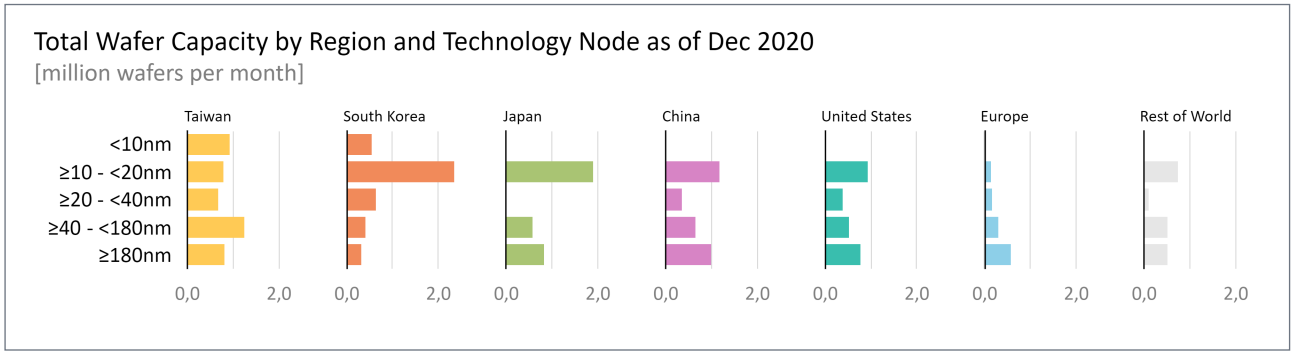

Figure 2

In summary, the EU has the smallest amount of total wafer capacity by far compared to other important regions in the semiconductor value chain, such as Japan, South Korea, Taiwan, United States or even China. Furthermore, only a tiny portion of that capacity can be used to manufacture modern logic semiconductors: Globalfoundries' 22nm FDSOI fab in Dresden and STMicroelectronics' 28nm FDSOI fab in Crolles, France. Infineon, NXP and STMicroelectronics are among the leading microcontroller suppliers for industrial and automotive applications[44]; however, most of these chips are manufactured at foundries. Thus, the majority of logic semiconductor suppliers follow a "fab-lite" business model and rely on foundries outside Europe.

That the major European IDMs did not focus on "More Moore Scaling" is also reflected in the spending on equipment over the past 20 years (**figure 3**). To keep pace with improving manufacturing processes, fabs must constantly expand capacity and invest in the next generation of manufacturing equipment. Thus, the amount of equipment spending per region is a good proxy to analyze which regions have seen the largest fab investments. In 2003, Europe was responsible for nearly 12% of all equipment spending, but in 2020, only 3% of equipment spending was in Europe. The global equipment market grew from US$22 billion in 2003 to around US$69 billion in 2020, but investment in manufacturing equipment in Europe was smaller in 2020 (US$2.4 billion) than in 2003 (US$2.56 billion).

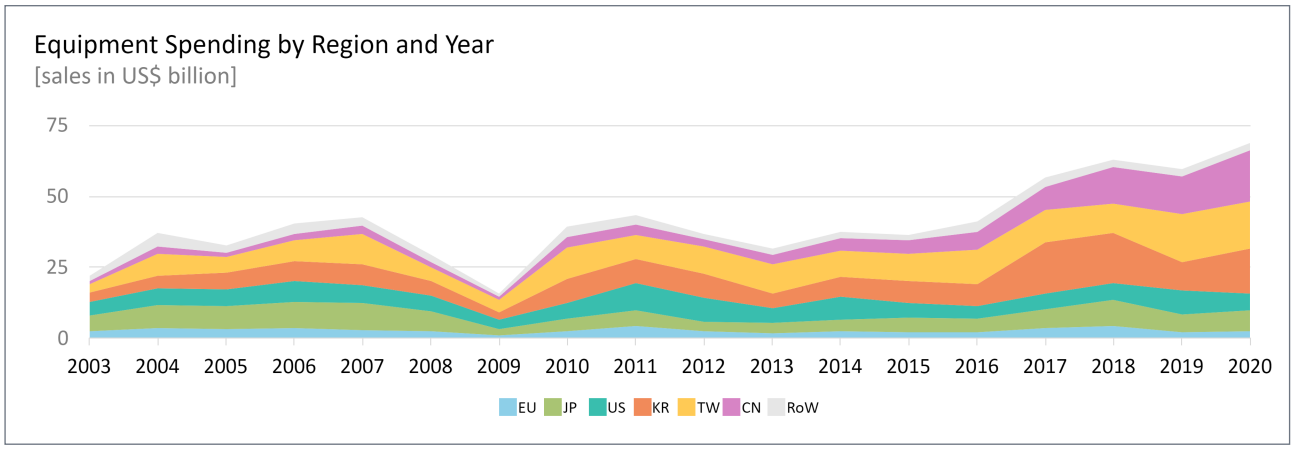

Figure 3

Figure 4 furthermore illustrates the long-term trend of cutting-edge wafer fabrication moving to Asian countries due to economies of scale, government incentives and market consolidation because of the economics of "More Moore Scaling." In 2003, Europe, Japan and United States together were responsible for nearly 60% of all equipment spending. By 2020, this number had decreased to 23%. Over the same time period, the combined equipment spending by China, South Korea and Taiwan grew from around 32% (2003) to more than 73% (2020).

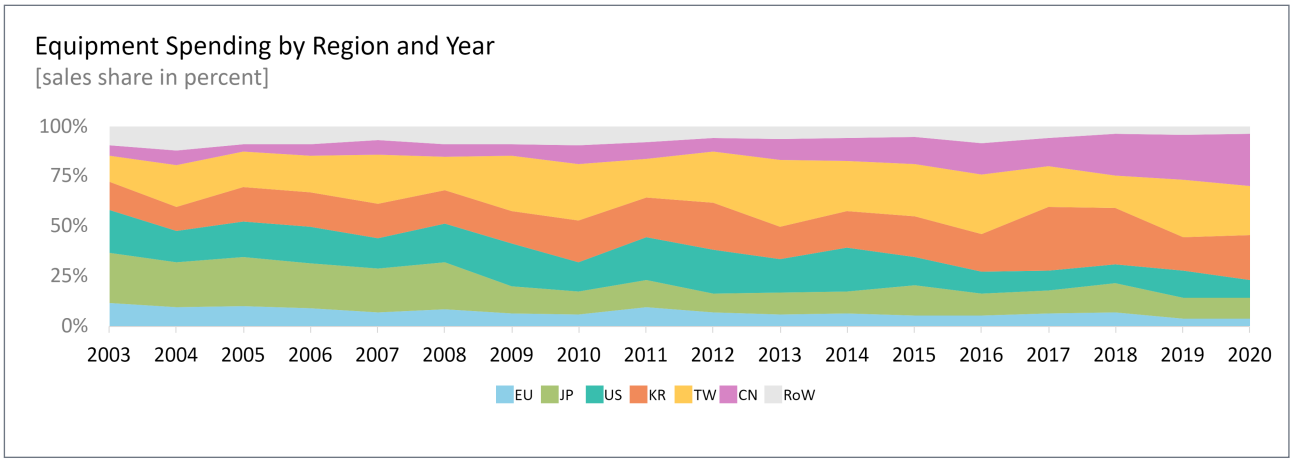

Figure 4

Did the leading European semiconductor companies simply underinvest in their own manufacturing capacity and thus, become increasingly dependent on foreign foundries? Not necessarily. Although European companies are certainly highly dependent on foreign foundries for logic semiconductors such as microcontrollers, some companies invested substantially in their own capacity. When comparing the capital expenditure (CAPEX) margin (CAPEX relative to revenue) with other leading analog semiconductor companies, there is no stark discrepancy (**figure 5**). Over the last 10 years, the CAPEX margin for analog semiconductor suppliers was between 3% and 15%. Naturally, companies that focus on "More Moore Scaling," such as Intel (15–25%) and TSMC (30–50%), have much higher CAPEX margins.

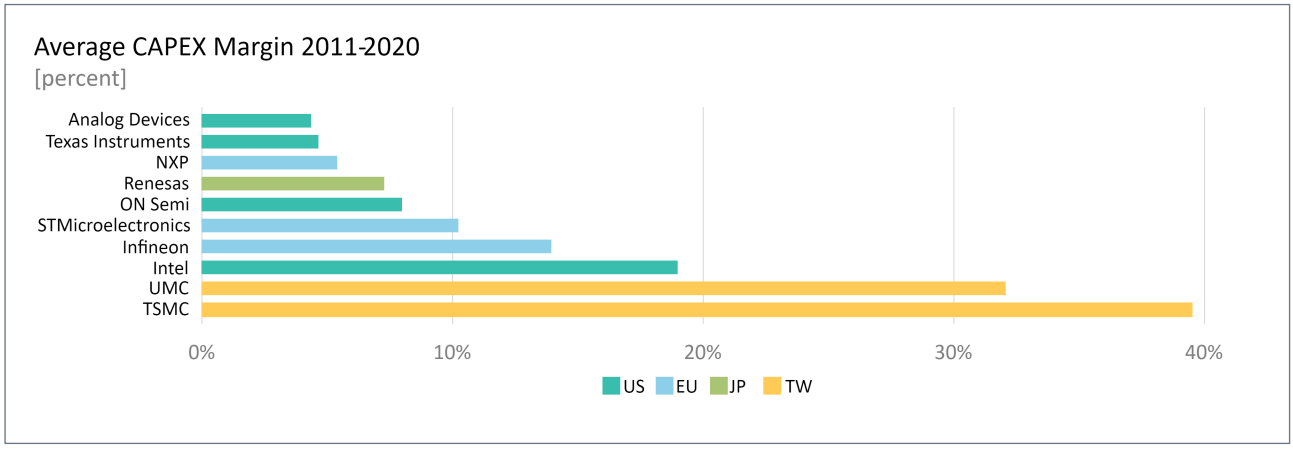

Figure 5

When upgrading old fabs or building new ones, European IDMs increasingly invested in compound semiconductors such as GaN and SiC. The physical properties of these compound materials provide substantial advantages over traditional silicon, especially for power semiconductors and radio frequency (RF) chips: from Bosch (SiC in Reutlingen, Germany) to Infineon (SiC/GaN in Villach, Austria)[45] and STMicroelectronics (SiC/GaN in Catania, Italy and GaN in Tours, France)[46]. As sensors, power and RF semiconductors are the strong suite of the EU's major semiconductor companies,

it is not surprising they invested in these "Beyond Moore" technologies instead of trying to further compete in silicon-based node shrinkage.

In summary, the substantial lack of wafer capacity for advanced logic semiconductors in Europe should not come as a surprise. European semiconductor suppliers focused on their customer base – mainly industrial and automotive – in terms of product differentiation. For both applications "More Moore Scaling" (raw compute power) was not an important factor. Furthermore, because of the lack of European consumer-facing electronics companies (the industry that relies on "More Moore Scaling" the most), there was simply no large-scale demand for advanced logic semiconductors. Of course, chips from European IDMs end up in consumer electronics but in small quantities and for sensing, power management or security applications, not logic. Of the 35 chips in Samsung's "Galaxy S20 Ultra 5G" smartphone, only two chips and two sensors are from European IDMs.[47] This lack of European consumer-facing electronics companies, combined with the economics of "More Moore Scaling" that created increasingly high barriers to enter cutting-edge wafer fabrication, led the EU's IDMs and foundries to invest less and less in advanced manufacturing capabilities for logic semiconductors. The companies simply did not benefit from node shrinkage for the vast majority of their products.

3. A cutting-edge EU foundry: in search of a business case

Because cutting-edge wafer fabrication is highly concentrated geographically (South Korea and Taiwan) and in terms of companies (Samsung and TSMC), debates within the EU about the need to invest in European cutting-edge wafer capacity to address potential geopolitical and geographic risks are increasing. The idea is that a 2–3nm foundry within the EU would diversify the market and secure capacity for European chip designers.[48] The European Commission's *2030 Digital Compass* clearly states the ambition to invest in cutting-edge fabs to rejuvenate the EU's semiconductor expertise.[49] Because of the steep barriers to enter the market of cutting-edge wafer fabrication and the substantial investments that would be necessary for such an endeavor, there has to be a strong business case for a cutting-edge foundry in the EU. In principal, there are three different ways to achieve that. The first strategy is convincing TSMC or Samsung through financial incentives to build a fab in the EU, as the US is doing. The second strategy is setting up an EU foundry (consortium) but licensing the process node technology from Samsung, similar to what Globalfoundries did for its 14nm nodes.[50] The third strategy is setting up an EU foundry that develops its own process node – the hardest and longest road.

For any of these strategies, there first must be a strong business case. However, there is not, mainly for two reasons: lack of cutting-edge chip design and ongoing efforts by the US to invest substantially in domestic wafer fabrication.

Lack of cutting-edge logic chip design in the EU

Only a handful of companies in the EU design chips on 5nm and 7nm process nodes, such as NXP[51], STMicroelectronics[52], mobile equipment vendor Ericsson and smaller start-ups like SiPearl (European Processor Initiative).[53] The following chart (**figure 6**) illustrates that EU chip designs play at best a marginal role in cutting-edge fabs. The forecast for the most important customers for wafer capacity at 5nm and 7nm globally clearly shows the dominance of US fabless companies.

The vast majority of capacity in 2021 will be used to manufacture chips for US-based companies such as AMD, Apple, Nvidia and Qualcomm. European chip designs can be found within *the Rest of Market (RoM)* category that will account for 6% (7nm) and 8% (5nm) of total wafer capacity in 2021. Of course, there are viable cutting-edge chip designs from NXP or the newly established European Processor Initiative (EPI),[54] but their order volumes in terms of wafer capacity simply does not register. Europe's problem starts on the demand side. Therefore, increasing supply

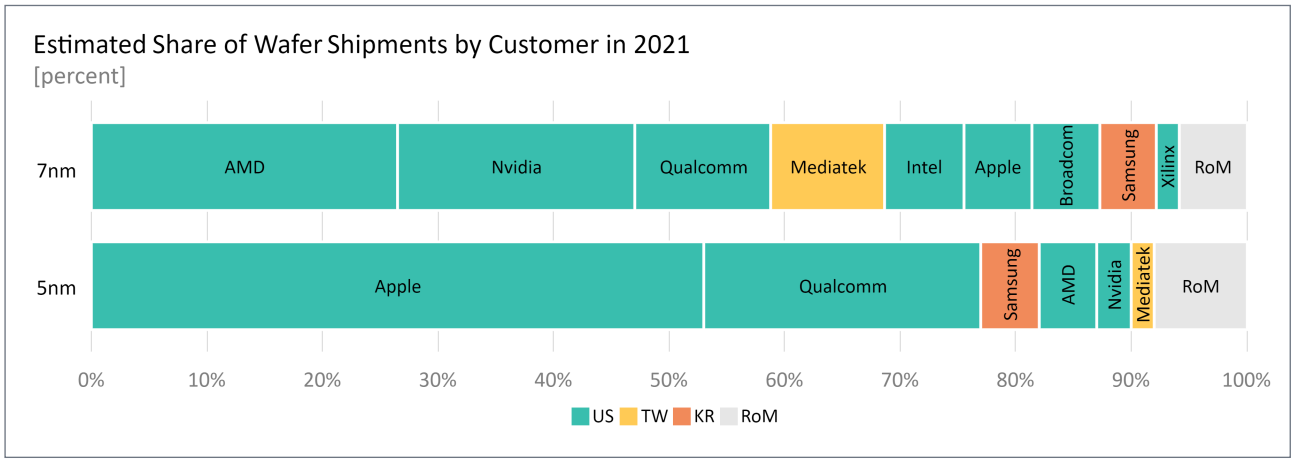

Figure 6

through an EU foundry before there is sufficient demand for cutting-edge wafer fabrication from European chip designers seems ill-advised.

TSMC and Samsung in the US

With the CHIPS for America Act, the United States wants to re-shore advanced wafer fabrication to lower the country's dependence on Taiwan and South Korea as global hubs for chip manufacturing.[55] Over the last few decades, many Asian countries established substantial financial incentives for chip manufacturing in the form of preferential loans, tax holidays and other subsidies.[56] The US wants to match these incentives, at least to some extent, to encourage foundries and IDMs to build new or upgrade older fabs in the US.[57] In 2020, TSMC announced it would build a new 5nm fab in Arizona,[58] and information about Samsung building a cutting-edge fab in the US leaked this year.[59] Samsung is asking for around US$1 billion in tax abatements and tax breaks.[60]

The US government's focus on wafer fabrication could be an economically viable strategy, because the US has the largest chip design industry in the world to create demand for these future fabs. All the subsidies in the world would not help to establish a sustainable wafer fabrication ecosystem if there were no demand.

The same is not the case for a potential EU foundry, however. Because of the lack of cutting-edge chip designs within Europe, the region would rely on foreign (US) chip design companies for orders. The question is, why would US fabless companies choose to manufacture their chips not in South Korea, Taiwan or the United States but in Europe? And why when the future cutting-edge EU fab is operated not by Samsung or TSMC but by an EU consortium[61]? A chip design is always based on a particular process node from a certain company's fab. One cannot simply switch from TSMC's 5nm node to Samsung's 5nm node. If TSMC or Samsung operates cut-

ting-edge fabs in the EU, they would most likely be compatible with the companies' existing process nodes. Meaning, the same chip design could potentially be manufactured in Taiwan, the US and EU (TSMC) or South Korea, the US and the EU (Samsung). In the case of an EU consortium, chip designs could be manufactured only at that fab. This makes it even more unlikely that non-European chip design companies would base their designs solely on the process node of a single EU foundry.

Furthermore, access to cutting-edge fabs in the US also changes the national security rationale for Europe. If sourcing chips solely from Taiwan or South Korea poses national security and business continuity risks, those risks could most likely be alleviated by sourcing the chips from the United States.

In summary, the US government's efforts to strengthen wafer fabrication in the US are backed by the US industry's substantial chip design capabilities. The same is simply not true for the EU. The EU lacks chip design capabilities for advanced logic semiconductors. Thus, a future EU foundry would need to attract non-EU customers. This is highly unlikely, especially in light of the cutting-edge fabs in the US announced by TSMC and Samsung and if Intel establishes its foundry business in the future.

Would an EU foundry have lessened the automotive chip shortage?

The automotive chip shortage was based on the interplay of three dynamics. The first was an overly pessimistic forecast by car manufacturers for how quickly the automotive market would recover from the pandemic. The second is the dominance of just-in-time delivery across the entire automotive supply chain leading to car manufacturers and tier-1 and tier-2 suppliers having essentially no inventory. The third is the simultaneously strong demand for consumer electronics due to employees working from home.

The first dynamic meant that car makers and their tier-1 suppliers (companies such as Continental, Bosch and Denso) stopped ordering chips in the second and third quarters of 2020. Thus, automotive tier-2 suppliers (semiconductor manufacturers such as Infineon, NXP and Renesas) saw demand drop significantly.[62] When the market recovered more quickly than expected, the second dynamic (no inventory due to just-in-time delivery) meant tier-1 suppliers almost immediately ran out of chips and had to reorder. Manufacturing a chip takes four to six months: wafer fabrication alone takes around three months, and then it must be assembled, tested and packaged.[63] To make things worse, automotive suppliers ordered chips when the fabs were already running at full capacity to produce chips for consumer electronics and cloud providers.[64]

In that situation, an EU foundry would have helped only if (1) automotive chip suppliers already used this particular fab for their designs and (2) if the foundry reserved some of its capacity for automotive customers. The latter is highly unlikely as consumer electronics required a lot of capacity, and an EU foundry would have also served those customers, because fabs are economically viable only under high utilization rates.

Thus, the automotive chip shortage is not a viable case to meaningfully argue in favor of increased wafer capacity within the EU, let alone for cutting-edge logic fabs. The majority of automotive chips are based on mature process nodes, not cutting-edge manufacturing.

4. Why the EU needs to invest in chip design first

Logic chips that depend on "More Moore Scaling" are often produced through the collaboration of fabless companies and foundries. The former focuses on innovations in chip design and the latter on investing in the manufacturing process. Today, fabless companies account for nearly 33% of global IC sales, up from 9% in 2000.[65] European IDMs rely on foundries for many of their logic chips because of this more cost-efficient division of labor.[66]

With a 65% market share the US has the largest fabless industry by far.[67] Many of the leading fabless companies, from AMD to Nvidia and Qualcomm, focus on "More Moore Scaling." Because fabless companies can focus completely on chip design, they have one of the highest R&D margins in the semiconductor industry, often 20–30% and higher. The following chart (**figure 7**) shows the accumulated R&D investments over the last 10 years for the 10 largest, publicly listed fabless companies. This R&D activity allows US fabless companies to stay at the cutting edge and develop increasingly more complex and sophisticated logic chips.

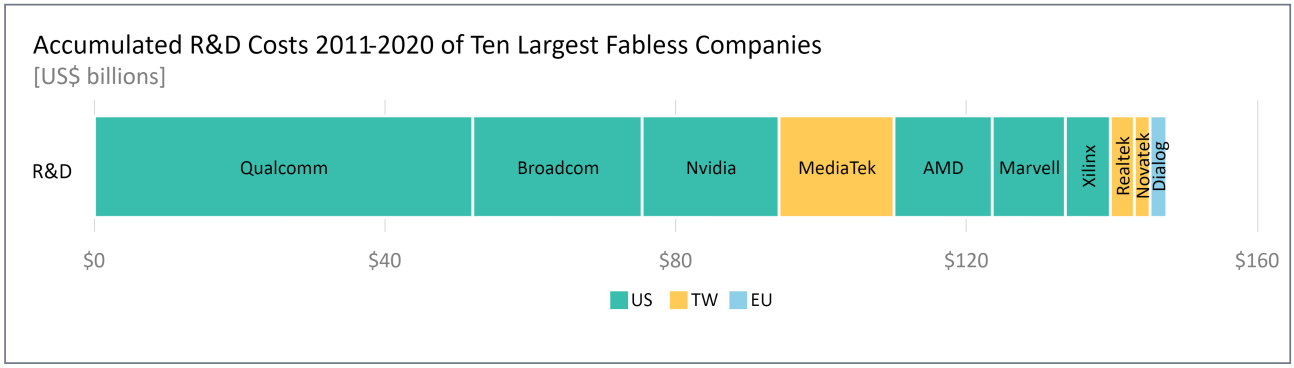

Figure 7

Over the same time period, Europe's fabless industry fell from 4% market share in 2010[68] to 2% in 2020.[69] Only two publicly listed fabless companies are left in Europe: Dialog Semiconductor (headquartered in the United Kingdom) and Nordic Semiconductors (headquartered in Norway). With the announcement of the acquisition of Dialog Semiconductor, the largest fabless company in Europe, by Renesas in Japan, this downward trend will most likely continue.[70]

The need to strengthen the EU's chip design capabilities and fabless industry was identified in 2013. The European Commission, with the industry, planned to "work on reinforcing its electronics design industries and fabless semiconductor companies."[71] In 2018, the European Commission again planned to strengthen the EU's chip design ecosystem through a "European Design Alliance" and "strategic design initiatives."[72] Instead, the EU's fabless industry shrunk by 50% over the last 10 years. Even worse, the European Commission's newest 10-year plan on digitalization, *2030 Dig-*

ital Compass, focuses almost exclusively on manufacturing and lacks a clear vision for chip design investment.[73]

If the EU does not create demand for cutting-edge wafer fabrication by significantly strengthening its chip design ecosystem (from universities to start-ups and verticals), investing in cutting-edge fabs will be a futile effort.

Conclusion

The continued focus on cutting-edge wafer fabrication in the EU's efforts to strengthen its technological sovereignty in semiconductors is ill-advised.[74] Investing in advanced logic fabs without a viable business case will very likely waste billions of public and private money. Yes, the EU completely lacks cutting-edge fabs, but more importantly, it lacks **design capabilities for advanced logic chips and a fabless industry**. Increasing supply (fabs) before there is demand within the EU (fabless companies) is at best overly optimistic and at worst naïve. Hoping that non-EU companies will base their designs on EU process nodes is highly unlikely, especially in light of the announcements that TSMC and Samsung plan to build cutting-edge fabs in the US. Furthermore, if Intel offers its foundry services in its existing fabs in Ireland, Europe potentially has access to trailing-edge fabs within this decade. At least at the moment, this scenario seems more likely than a greenfield fab investment by TSMC in the EU.[75]

The EU has world-class RTOs, equipment suppliers and silicon wafer vendors that are all deeply involved in cutting-edge wafer fabrication in South Korea, Taiwan and the United States. But Europe's own semiconductor industry predominantly designs logic chips on trailing-edge and mature process nodes, for industrial and automotive applications. Thus, if the EU wants to invest in fabs today, these investments should focus on **trailing-edge wafer fabrication at 14nm and above**.

However, Europe's key problem is not just wafer fabrication but advanced logic chip design. Yet in the joint declaration from December 2020, chip design plays only an ancillary role[76] and even a smaller role in the *2030 Digital Compass*. European governments are right to look more closely at the competitiveness and dependencies of our own semiconductor industry. But the strong focus on a 2nm fab is ill-advised and will waste money, resources and attention while there is a much bigger problem at hand.

List of figures

Figure 1: **Total Wafer Capacity by Region (2010, 2015, 2020)** (data: IC Insights)

	2010	2015	2020
TW	2,66	3,547	4,45
KR	1,88	3,357	4,25
JP	2,71	2,824	3,28
CN	1,04	1,591	3,18
US	1,81	2,32	2,62
EU	1	1,046	1,18
RoW	1,25	1,665	2

Figure 2: **Total Wafer Capacity by Region and Technology Node** (data: IC Insights, https://semiwiki.com/forum/index.php?attachments/monthly-wafer-capacity-2020-icinsights-jpg.350/)

	≥180nm	<180nm–≥40nm	<40nm–≥20nm	<20nm–≥10nm	<10nm
EU	0,58	0,31	0,16	0,13	0,00
JP	0,82	0,57	0,00	1,89	0,00
US	0,77	0,53	0,39	0,93	0,00
TW	0,81	1,24	0,68	0,80	0,93
KR	0,32	0,40	0,63	2,34	0,55
CN	0,98	0,66	0,36	1,18	0,00
RoW	0,52	0,51	0,09	0,73	0,00

Figure 3 and 4: **Equipment Spending by Region and Year** (data: SEMI)

	2003	2004	2005	2006	2007	2008	2009	2010	2011
EU	2,56	3,44	3,26	3,6	2,94	2,45	0,97	2,33	4,22
KR	3,12	4,51	5,83	7,01	7,35	4,89	2,6	8,33	8,66
TW	2,92	7,76	5,72	7,32	10,65	5,01	4,35	11,19	8,52
CN	1,16	2,68	1,33	2,31	2,92	1,89	0,94	3,63	3,65
US	4,73	5,81	5,7	7,32	6,55	5,63	3,39	5,76	9,26
JP	5,56	8,28	8,18	9,21	9,31	7,04	2,23	4,44	5,81
RoW	2,1	4,49	2,88	3,71	3,05	2,61	1,44	3,85	3,41
Σ	22,15	36,97	32,9	40,48	42,77	29,52	15,92	39,53	43,53

	2012	2013	2014	2015	2016	2017	2018	2019	2020F
EU	2,55	1,91	2,38	1,94	2,18	3,67	4,22	2,27	2,4
KR	8,67	5,13	6,84	7,47	7,69	17,95	17,71	9,97	15,7
TW	9,53	10,57	9,41	9,64	12,23	11,49	10,17	17,12	16,8
CN	2,5	3,27	4,37	4,9	6,46	8,23	13,11	13,45	18,1
US	8,15	5,26	8,16	5,12	4,49	5,59	5,83	8,15	6,1
JP	3,42	3,38	4,18	5,49	4,63	6,49	9,47	6,27	7,3
RoW	2,1	2,07	2,15	1,97	3,55	3,2	2,52	2,52	2,6
Σ	36,92	31,59	37,49	36,53	41,23	56,62	63,03	59,75	69

Figure 5: **Average CAPEX Margin 2011–2020** (data: quarterly company financial data)

Figure 6: **Estimated Wafer Shipments by Customer in 2021** (data: Counterpoint, https://www.counterpointresearch.com/foundry-industry-revenue-growth-continue-2021/)

Figure 7: **Accumulated R&D Costs 2011–2020 of the Ten Largest Fabless Companies** (data: quarterly company financial data)

References

1 Alex Capri. 2020. "Semiconductors at the Heart of the US-China Tech War". Hinrich Foundation. https://hinrichfoundation.com/trade-research/global-trade-research/thought-leadership/semiconductors-at-the-heart-of-the-us-china-tech-war/

2 Ross Seymore, et al. 2018. "DB Semiconductor Industry Primer". Deutsche Bank Research.

3 Andrea Peterson. 2021. "New Microelectronics Initiative Sets Up Possible Funding Infusion". American Institute of Physics. https://www.aip.org/fyi/2021/new-microelectronics-initiative-sets-possible-funding-infusion

4 Semiconductor Industry Association. 2020. "SIA Factbook 2020". https://www.semiconductors.org/the-2020-sia-factbook-your-source-for-semiconductor-industry-data/

5 European Commission. 2020. "Declaration: A European Initiative on Processors and semiconductor technologies". https://ec.europa.eu/newsroom/dae/document.cfm?doc_id=73940

6 European Commission. 2021. "2030 Digital Compass: the European way for the Digital Decade". COM(2021) 118 final. https://ec.europa.eu/info/sites/info/files/communication-digital-compass-2030_en.pdf

7 European Commission. 2020. "Member States join forces for a European initiative on processors and semiconductor technologies". https://ec.europa.eu/digital-single-market/en/news/member-states-join-forces-european-initiative-processors-and-semiconductor-technologies

8 Jan-Peter Kleinhans, Nurzat Baisakova. 2020. "The Global Semiconductor Value Chain: A Technology Primer for Policy Makers". Stiftung Neue Verantwortung. https://www.stiftung-nv.de/sites/default/files/the_global_semiconductor_value_chain.pdf

9 Synopsys. 2020. "Synopsys Collaborates with TSMC to Accelerate 3nm Innovation, Enabling Next-Generation SoC Design". https://news.synopsys.com/2020-08-25-Synopsys-Collaborates-with-TSMC-to-Accelerate-3nm-Innovation-Enabling-Next-Generation-SoC-Design

10 Cheng Ting-Fang, Lauly Li. 2021. "TSMC supplier LCY to build US plant as chip supply chain shifts". Nikkei Asia. https://asia.nikkei.com/Business/Tech/Semiconductors/TSMC-supplier-LCY-to-build-US-plant-as-chip-supply-chain-shifts

11 ASML. 2020. "ASML unveils EUV Technology Training Center in Taiwan". https://www.asml.com/en/news/press-releases/2020/asml-unveils-euv-technology-training-center-in-taiwan

12 Joel Hruska. 2021. "Apple, TSMC On Track to Move 3nm Into Risk Production by the End of 2021". ExtremeTech. https://www.extremetech.com/computing/320460-apple-tsmc-on-track-to-move-3nm-into-risk-production-by-the-end-of-2021

13 Scotten Jones. 2021. "ISS 2021 – Scotten W. Jones – Logic Leadership in the PPAC era". SemiWiki. https://semiwiki.com/events/294639-iss-2021-scotten-w-jones-logic-leadership-in-the-ppac-era/

14 McKinsey & Company. 2020. "Semiconductor design and manufacturing: Achieving leading-edge capabilities". https://www.mckinsey.com/industries/advanced-electronics/our-insights/semiconductor-design-and-manufacturing-achieving-leading-edge-capabilities

15 Kif Leswing. 2021. "Apple reports blowout quarter, booking more than $100 billion in revenue for the first time". CNBC. https://www.cnbc.com/2021/01/27/apple-aapl-earnings-q1-2021.html

16 IC Insights. 2020. "Texas Instruments Maintains Firm Grip As World's Top Analog IC Supplier". https://www.icinsights.com/news/bulletins/Texas-Instruments-Maintains-Firm-Grip-As-Worlds-Top-Analog-IC-Supplier/

17 IC Insights. 2021. "Top Five Wafer Capacity Leaders Raise Share of Global Capacity to 54%". https://www.icinsights.com/news/bulletins/Top-Five-Wafer-Capacity-Leaders-Raise-Share-Of-Global-Capacity-To-54/

18 Dale Gai. "A Mega Wave of Capex Cycle Starts in Logic Semiconductor Industry". Counterpoint. https://www.counterpointresearch.com/mega-wave-capex-cycle-logic-semiconductor-industry/

19 Anton Shilov. 2021. "Samsung Foundry: New $17 Billion Fab in the USA by Late 2023". AnandTech. https://www.anandtech.com/show/16483/samsung-in-the-usa-a-17-billion-usd-fab-by-late-2023

20 Antonio Varas, Raj Varadarajan, Jimmy Goodrich, Falan Yinug. 2020. "Government Incentives and US Competitiveness in Semiconductor Manufacturing". Boston Consulting Group. https://www.bcg.com/publications/2020/incentives-and-competitiveness-in-semiconductor-manufacturing

21 McKinsey & Company. 2020. "Semiconductor design and manufacturing: Achieving leading-edge capabilities". https://www.mckinsey.com/industries/advanced-electronics/our-insights/semiconductor-design-and-manufacturing-achieving-leading-edge-capabilities

22 Hannah Chang, Liang-rong Chen. 2020. "Does Taiwan Have Enough Power for TSMC?". CommonWealth Magazine. https://english.cw.com.tw/article/article.action?id=2766

23 UMC. 2021. "UMC Reports Fourth Quarter 2020 Results". https://www.umc.com/upload/media/08_Investors/Financials/Quarterly_Results/Quarterly_2020-2029_English_pdf/2020/Q4_2020/UMC20Q4_report.pdf

24 Dale Gai. 2021. "Foundry Industry's Robust Revenue Growth to Continue in 2021". Counterpoint. https://www.counterpointresearch.com/foundry-industry-revenue-growth-continue-2021/

25 Mark Patel, et al. 2016. "Ramping up at warp speed". McKinsey & Company. https://www.mckinsey.com/industries/semiconductors/our-insights/ramping-up-at-warp-speed

26 Mark Lapedus. 2021. "New Transistor Structures At 3nm/2nm". SemiEngineering. https://semiengineering.com/new-transistor-structures-at-3nm-2nm/

27 Joel Hruska. 2020. "Intel Urged to 'Explore Alternatives' to Manufacturing Its Own Chips". ExtremeTech. https://www.extremetech.com/computing/318734-activist-firm-urges-intel-to-explore-alternatives-to-manufacturing-its-own-chips
28 Ian Cutress, 2021. "Intel's New IDM 2.0 Strategy: $20b for Two Fabs, Meteor Lake 7nm Tiles, New Foundry Services, IBM Collaboration, Return of IDF". AnandTech. https://www.anandtech.com/show/16573/intels-new-strategy-20b-for-two-fabs-meteor-lake-7nm-tiles-new-foundry-services-ibm-collaboration-return-of-idf
29 Scotten Jones. 2021. "Intel's IDM 2.0". SemiWiki https://semiwiki.com/semiconductor-manufacturers/intel/297403-intels-idm-2-0/
30 Anton Shilov. 2020. "SMIC: Advanced Process Technologies and Gov't Funding (Part 2)". EETimes. https://www.eetimes.com/smic-advanced-process-technologies-and-govt-funding-part-2/
31 Scotten Jones. 2021. "IEDM 2020 – Imec Plenary talk". SemiWiki. https://semiwiki.com/events/294432-iedm-2020-imec-plenary-talk/
32 Scotten Jones. 2021. "ISS 2021 – Scotten W. Jones – Logic Leadership in the PPAC era". SemiWiki. https://semiwiki.com/events/294639-iss-2021-scotten-w-jones-logic-leadership-in-the-ppac-era/
33 Antonio Varas, Raj Varadarajan, Jimmy Goodrich, Falan Yinug. 2020. "Government Incentives and US Competitiveness in Semiconductor Manufacturing". Boston Consulting Group. https://www.bcg.com/publications/2020/incentives-and-competitiveness-in-semiconductor-manufacturing
34 Intel. 2019. "Form 10-K". https://www.intc.com/filings-reports/annual-reports/content/0000050863-19-000007/0000050863-19-000007.pdf
35 Eamonn Sinnott. 2021. "Intel Shares Europe's 2030 Digital Ambition". Euractiv. https://www.euractiv.com/section/digital/opinion/intel-shares-europes-2030-digital-ambition/
36 STMicroelectronics. 2019. "Manufacturing Strategy". Presentation Capital Markets Day. https://stmicroelectronics-nv.gcs-web.com/static-files/8d0bbcfb-c179-4ed8-8d21-7f7b423e8ac6
37 Fully depleted silicon-on-insulator (FD-SOI) is an alternative manufacturing technology resulting in energy-efficient chips. Several companies in the EU specialize in SOI, such as STMicroelectronics, SOITEC (wafer), CEA-Leti (research) and Globalfoundries.
38 Anton Shilov. 2020. "GlobalFoundries Offers Ambitious Tech Plans, While Eying an IPO". EETimes. https://www.eetimes.com/globalfoundries-offers-ambitious-tech-plans-while-eying-an-ipo/
39 Marc Sauter. 2019. "Ein Blick in Boschs 300-mm-Fab". Golem. https://www.golem.de/news/rb300-ein-blick-in-boschs-300-mm-fab-1910-144314-2.html
40 Infineon. 2013. "First Quarter FY 2013". Investor Relations Presentation. https://www.infineon.com/dgdl/2013_01_31_Q1_FY13_Investor_Presentation.pdf?fileId=db3a30433c8a9179013c8f713062568c
41 NXP. 2020. "Annual Report 2019". https://investors.nxp.com/static-files/dd317bc2-1235-467f-b072-0d5ab34194ed
42 XFab. NN. "Our Fabs". https://www.xfab.com/manufacturing/our-fabs
43 United Monolithic Semiconductors. NN. "Technologies". https://www.ums-rf.com/foundry/technologies/
44 STMicroelectronics. 2020. "Microcontrollers & Digital ICs Group Presentation". Presentation Capital Markets Day 2020. https://investors.st.com/static-files/282253bb-9979-463e-a61a-32214023324a
45 Infineon. 2018. "IFX Day 2018". Presentation Jochen Hanebeck. https://www.infineon.com/dgdl/IFX+Day++2018+-+COO.pdf?fileId=5546d46163a777860163ef2da3a40056
46 STMicroelectronics. 2020. "STMicroelectronics Capital Markets Day – 2020 Strategic Update". Presentation. https://investors.st.com/static-files/8b6b07fd-2e5a-451a-9bc2-c164a7d801a4
47 Daniel Yang, Ray Fontaine. NN. "Samsung Galaxy S20 Ultra 5G Teardown Analysis". TechInsights. https://www.techinsights.com/blog/samsung-galaxy-s20-teardown-analysis
48 European Commission. 2020. "Speech by Commissioner Thierry Breton at Hannover Messe Digital Days". https://ec.europa.eu/commission/presscorner/detail/en/SPEECH_20_1362
49 European Commission. 2021. "2030 Digital Compass: the European way for the Digital Decade". COM(2021) 118 final. https://ec.europa.eu/info/sites/info/files/communication-digital-compass-2030_en.pdf
50 Globalfoundries. 2014. "Samsung and GLOBALFOUNDRIES Forge Strategic Collaboration to Deliver Multi-Sourced Offering of 14nm FinFET Semiconductor Technology". Press Release. https://www.globalfoundries.com/sites/default/files/samsung-globalfoundries-14nm-collaboration-press-release.pdf
51 Junko Yoshida. 2020. "NXP to Jump to TSMC's 5nm for Next-Gen Auto SoC Platform". EETimes. https://www.eetimes.com/nxp-to-jump-to-tsmcs-5nm-for-next-gen-auto-soc-platform/
52 Junko Yoshida. 2020. "New ICs Put ST in Robocar Race". EETimes. https://www.eetimes.com/new-ics-put-st-in-robocar-race/
53 HPCWire. 2020. "SiPearl Begins Development of European Processor with €6.2M". Press Release. https://www.hpcwire.com/off-the-wire/sipearl-begins-development-of-european-processor-with-e6-2m/
54 Nick Flaherty. 2021. „SiPearl teams for 6nm HPC chip". eeNews Europe. https://www.eenewseurope.com/news/sipearl-teams-6nm-hpc-chip
55 Mark Lapedus. 2020. "Regaining U.S. Chip Competitiveness". SemiEngineering. https://semiengineering.com/regaining-u-s-chip-competitiveness/
56 Semiconductor Industry Association. 2020. "US Needs Greater Semiconductor Manufacturing Incentives". https://www.semiconductors.org/wp-content/uploads/2020/07/U.S.-Needs-Greater-Semiconductor-Manufacturing-Incentives-Infographic.pdf

57 Antonio Varas, Raj Varadarajan, Jimmy Goodrich, Falan Yinug. 2020. "Government Incentives and US Competitiveness in Semiconductor Manufacturing". Boston Consulting Group. https://www.bcg.com/publications/2020/incentives-and-competitiveness-in-semiconductor-manufacturing
58 Jan-Peter Kleinhans. 2020. "TSMC prepares for US-China chips decoupling". TechNode. https://technode.com/2020/05/27/tsmc-prepares-for-us-china-chips-decoupling/
59 Anton Shilov. 2021. "Samsung Foundry: New $17 Billion Fab in the USA by Late 2023". AnandTech. https://www.anandtech.com/show/16483/samsung-in-the-usa-a-17-billion-usd-fab-by-late-2023
60 ibid.
61 Paul van Gerven. 2021. "The only way Europe is getting that leading-edge fab". Bits&Chips. https://bits-chips.nl/artikel/the-only-way-europe-is-getting-that-leading-edge-fab/
62 Douglas Busvine, Christoph Steitz. 2021. "Analysis: Carmakers wake up to new pecking order as chip crunch intensifies". Reuters. https://www.reuters.com/article/us-autos-chips-analysis-idUSKBN2AJ0LD
63 Falan Yinug. 2021. "Chipmakers Are Ramping Up Production to Address Semiconductor Shortage. Here's Why that Takes Time". Semiconductor Industry Association. https://www.semiconductors.org/chipmakers-are-ramping-up-production-to-address-semiconductor-shortage-heres-why-that-takes-time/
64 Bindiya Vakil, Tom Linton. 2021. "Why We're in the Midst of a Global Semiconductor Shortage". Harvard Business Review. https://hbr.org/2021/02/why-were-in-the-midst-of-a-global-semiconductor-shortage
65 IC Insights. 2020. "Fabless Company Share of IC Sales to Set New Record in 2020 at 32.9%". https://www.icinsights.com/news/bulletins/Fabless-Company-Share-Of-IC-Sales-To-Set-New-Record-In-2020-At-329-/
66 Namchul Shin, et al. 2017. "R&D and firm performance in the semiconductor industry". Industry and Innovation. https://doi.org/10.1080/13662716.2016.1224708
67 IC Insights. 2020. "U.S. IC Companies Maintain Global Marketshare Lead". https://www.icinsights.com/news/bulletins/US-IC-Companies-Maintain-Global-Marketshare-Lead/
68 IC Insights. 2018. "U.S. Companies Maintain Largest Share of Fabless Company IC Sales". https://www.icinsights.com/news/bulletins/US-Companies-Maintain-Largest-Share-Of-Fabless-Company-IC-Sales/
69 IC Insights. 2020. "U.S. IC Companies Maintain Global Marketshare Lead". https://www.icinsights.com/news/bulletins/US-IC-Companies-Maintain-Global-Marketshare-Lead/
70 Renesas. 2021. "Renesas and Dialog Semiconductor to Join Forces to Advance Global Leadership in Embedded Solutions". Press Release. https://www.renesas.com/br/en/about/press-room/renesas-and-dialog-semiconductor-join-forces-advance-global-leadership-embedded-solutions
71 European Commission. 2014. "A European Industrial Strategic Roadmap for Micro- and Nano-Electronic Components and Systems". https://ec.europa.eu/newsroom/dae/document.cfm?doc_id=4482
72 European Commission. 2018. "Boosting Electronics Value Chains in Europe". http://ec.europa.eu/newsroom/dae/document.cfm?doc_id=53119
73 European Commission. 2021. "2030 Digital Compass: the European way for the Digital Decade". COM(2021) 118 final. https://ec.europa.eu/info/sites/info/files/communication-digital-compass-2030_en.pdf
74 Laurens Cerulus, Jakob Hanke Vela. 2021. "Europe looks to go it alone on microchips amid US-China clash". Politico. https://www.politico.eu/article/europe-seeks-to-decouple-from-us-china-chip-war/
75 Kathrin Hille. 2021. "TSMC: how a Taiwanese chipmaker became a linchpin of the global economy". Financial Times. https://www.ft.com/content/05206915-fd73-4a3a-92a5-6760ce965bd9
76 European Commission. 2020. "Declaration: A European Initiative on Processors and semiconductor technologies". https://ec.europa.eu/newsroom/dae/document.cfm?doc_id=73940

About the Stiftung Neue Verantwortung

The Stiftung Neue Verantwortung (SNV) is an independent, non-profit think tank working at the intersection of technology and society. SNV's core method is collaborative policy development, involving experts from government, tech companies, civil society and academia to test and develop analyses with the aim of generating ideas on how governments can positively shape the technological transformation. To guarantee the independence of its work, the organization has adopted a concept of mixed funding sources that include foundations, public funds and corporate donations.

About the Author

Jan-Peter Kleinhans is director of the "Technology and Geopolitics" project. Currently his work focuses on the intersection of global semiconductor supply chains and geopolitics. Previously Jan-Peter worked on 5G security and presented his work at the German parliament's committee on foreign affairs and the NATO parliamentary assembly. After joining SNV in 2014 Jan-Peter analyzed why the market failed to produce reasonably trustworthy consumer IoT devices. He explored if and how standardization, certification and market surveillance can create economic incentives for IoT manufacturers to produce secure and trustworthy IoT devices. He is Fellow of the Transatlantic Digital Debates 2016 and studied communication sciences in Uppsala, Sweden and business informatics in Darmstadt.

Contact the Author:

Jan-Peter Kleinhans
jkleinhans@stiftung-nv.de

Imprint

Stiftung Neue Verantwortung e.V.
Beisheim Center
Berliner Freiheit 2
10785 Berlin

T: +49 (0) 30 81 45 03 78 80
F: +49 (0) 30 81 45 03 78 97

www.stiftung-nv.de
info@stiftung-nv.de

Design:
Make Studio
www.make-studio.net

Layout:
Jan Klöthe